A 4-Path 60GHz CMOS Phased-Array Receiver

by

WU Liang

A Thesis Submitted to
The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
the Degree of Doctor of Philosophy
in the Department of Electronic and Computer Engineering

August 2012

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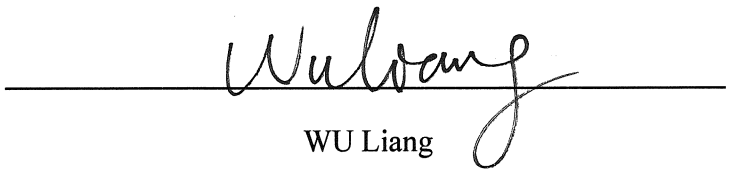

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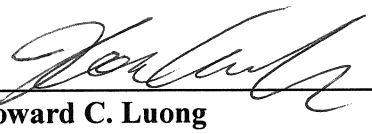

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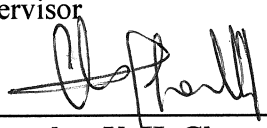

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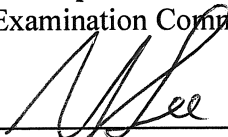

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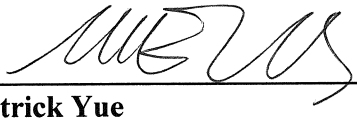

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Abstract

The 60-GHz worldwide unlicensed band provides up to 9-GHz bandwidth and thus enables Gb/s-data-rate point-to-point communication links and high-definition video transfer. However, implementations of circuits and systems at this frequency range are still quite challenging. This dissertation is dedicated to the design and demonstration of a high-performance 4-path 60-GHz phased-array receiver front-end (RFE) in CMOS technology with novel ideas at both system architecture and circuit implementation.

At the circuit level, several novel design techniques for the key building blocks were demonstrated. First, a 24-GHz and 60-GHz dual-band standing-wave VCO with mode-switching technique was designed in 0.13μm CMOS process. Second, a bimodal transformer-based enhanced magnetic tuning technique was proposed to implement a quadrature VCO (QVCO) in 65nm CMOS process with an ultra-wide frequency tuning range from 48.8 GHz to 62.3 GHz (corresponding to 24 % tuning range at 60GHz) and figure-of-merit (FoM) of 181 to 184 dBc. Third, to operate the QVCO in a phased-lock loop (PLL), a harmonic-boosting technique with 4^{th}-order LC tank was proposed to achieve a divide-by-4 injection-locked frequency divider with state-of-the-art frequency

locking range (LR) from 58.5 GHz to 72.9 GHz (21.9 % at 60GHz) and figure-of-merit (FoM) of 6.5 GHz/mW.

Furthermore, an LO generation scheme was proposed to generate LO signals with required phase shifts for a 4-path phased-array receiver. Circuit techniques include highly linear phase shifters, wide-locking-range frequency tripler, and successive-approximation phase tuning algorithm. Implemented in 65nm CMOS, the LO generation measures linear phase range larger than -90 ° ~ 90 °, amplitude variation less than ±0.35dB, phase resolution of 22.5 °, and phase error smaller than 1.5 °.

Finally, at the system level, a 4-path phased-array receiver front-end system was designed and integrated in a 65-nm CMOS process. With proposed hybrid-mode mixing scheme, the system performance (in terms of linearity, noise figure, gain, power consumption, and chip area) is significantly improved as compared to existing solutions. In addition, modified successive algorithm is proposed for automatic phase calibration and gain equalization to achieve beam-forming with maximum peak-signal-to-noise ratio of more than 28dB.

Chapter 1

Introduction

1.1 Background

Over the last decade, wireless communication at several-GHz frequency bands has experienced explosive growth that the available frequency spectrum becomes very limited. Recently, a great deal of interest from academia, industry and standardization bodies is being attracted to higher frequency bands even at millimeter-wave (mm-Wave) region where wide channel bandwidth can be provided to enable high data rate communications. The 60-GHz band has some advantages compared to other unlicensed bands. The available bandwidth is up to 9 GHz and has been allocated in most countries, as summarized in Fig. 1.1. Thanks to the large path loss at mm-Wave frequency, not

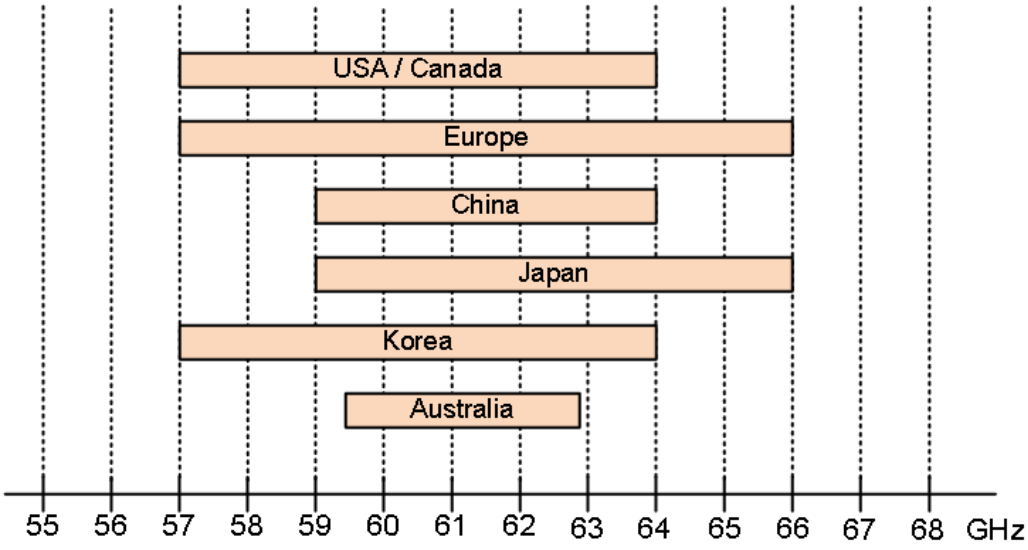

Fig. 1.1 Bandwidth allocation of 60-GHz unlicensed band

only the transmission power level is less restricted [1], but also secure communication can be obtained, which is important when there are multiple networks close to each other, as show in Fig. 1.2. The great potential in terms of capacity and flexibility makes it fascinated for gigabit wireless applications. Particularly, IEEE standard 802.15.3c is on the way and many new applications are enabled [2], including short-range wireless links with data rate up to 5 Gb/s and high-definition video transmission [3], as shown in Fig. 1.3.

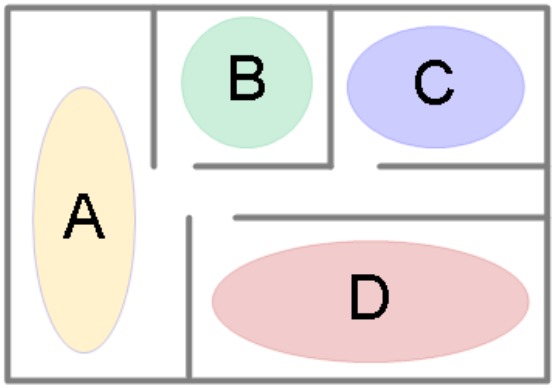

Fig. 1.2 Secure communication of multiple wireless personal area networks (WPANs)

Fig. 1.3 60-GHz wireless applications

However, mm-Wave communications face a number of important challenges spanning a broader range of topics that must be solved, including wave propagation, channel model, circuit design and antenna implementation. From the circuit point of view, this ultra-high frequency obviously requires high-speed active devices. Besides, the large path loss and atmosphere absorption demand transmitter with high output power and receiver with good sensitivity. Conventionally, only compound semiconductor technologies, such as gallium arsenide (GaAs) and indium phosphide (InP), can be utilized to fulfill those requirements. But their high cost is an obstacle for consumer market spreading of mm-Wave applications.

With recent advancement in nanometer scale silicon-based technology, the transition frequency (f_T) of transistor exceeds 100 GHz, making the implementation of mm-Wave circuits in CMOS possible. Compared with compound semiconductor, CMOS solution is cheaper and offers the opportunity to realize 60-GHz system-on-chip (SoC) with RF front-end, analog baseband, digital signal processing, calibration and self-testing integrated. Thanks to the small wavelength at mm-Wave frequencies, the size of the antennas is small and can be in package [4] or on chip [5], which reducing or even eliminating the electrical interface at mm-Wave frequencies.

1.2 Research Motivation

Despite various advantages of CMOS technology, there are some challenges to fully integrate mm-Wave system, from a single device to a circuit and finally to a system. The low breakdown voltage of transistors resulting from the scaling process and the shrinking of the depletion regions limits the achievable output power of power

amplifier. Silicon substrate is conductive for bulk processes and thus energy loss due to magnetically induced eddy currents is inevitably large. At higher frequency, the parasitics are more dominant, so the models of both active devices and passive components become less inaccurate, especially in the presence of process variations and environmental changes. Flicker noise increases as channel length being scaled down. From the aspect of circuit design, the performance of some critical building blocks especially in RF front-end, such as low-noise amplifier (LNA), mixer, power amplifier (PA), local oscillator (LO), frequency divider would be degraded if simply moving existing solutions at several GHz to 60-GHz. Therefore, new circuit techniques are urgently mandated. For the system, the transmitted power and receiver sensitivity need to be improved to fulfill the requirements of Gb/s communications.

One promising solution in system level is spatial power combing provided by phased-array. On transmitter side, phased-array combines power from multiple transmitters and thus can help to achieve sufficient output power for the system. On receiver side, phased-array can improve the signal noise ratio (SNR) by 10logN compared with single receiver theoretically, where N is the element number. In addition, the phase-array system is able to perform beam steering and thus features spatial selectivity to improve spectral efficiency by suppressing unwanted signals, which come from nearby devices and might be very strong.

1.3 Objective of the Dissertation

In this dissertation, the objection is on the design and implementation of a 4-path 60-GHz phased-array receiver front-end in CMOS technology. The dissertation is organized as follows:

Chapter 2 investigates the system specification of IEEE 802.15.3c standard. Based on different channel models, the link budget is calculated for both basic transceiver and phased-array transceiver.

Chapter 3 discusses system architectures, including both basic receiver and phased-array receiver, in order to make the performance trade-offs well understood. Based on dual-conversion zero-IF architecture, the detailed specifications of each building block are derived.

Chapter 4 presents a 60-GHz LC-type injection-locked frequency divider-by-4. Based on theoretical analysis, third-order harmonic boosting technique implemented with a 4^{th}-order LC tank is proposed to significantly enhance the injection efficiency and thus the locking range.

Chapter 5 presents a 60-GHz QVCO with ultra-wide frequency tuning range. After the investigation and theoretical analysis of existing frequency tunings, a novel tuning mechanism named bimodal enhanced magnetic tuning is proposed and experimentally validated.

Chapter 6 discusses a 24-GHz and 60-GHz dual-band VCO based on standing-wave oscillator (SWO), which is a potential solution to generate LO signals for

multiple-band mm-Wave transceiver. The associated circuit implementation and stability analysis issues are addressed and validated.

Chapter 7 focuses on the LO generation with phase shift for targeted 60-GHz phased-array receiver. Linear phase shift is achieved with proposed injection-locked phase shifter cascaded with injection-locked frequency tripler. A novel successive-approximation algorithm is proposed to automatically detect and tune the LO phase difference specified by the system.

Chapter 8 presents the whole integrated 4-path phased-array receiver system. With the theoretical investigation on existing voltage-mode and current-mode RF front-ends, a new hybrid-mode mixing topology is proposed, designed, analyzed and experimentally verified. Another key feature, automatic beamforming is realized by sequentially equalizing the gain and tuning the phase with a close-loop.

Chapter 9 summarizes the research work and the contributions of the dissertation.

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Chapter 2

System Specification

2.1 Specification of IEEE 802.15.3c [1]

2.1.1 Overview

The IEEE 802.15.3c standard is targeted at supporting 60-GHz wireless communications with data rate of gigabit per second (Gb/s) over a few meters. The specification defines a total of three physical layers (PHYs), namely single carrier (SC) PHY, high speed interface (HSI) orthogonal frequency division multiplexing (OFDM) PHY and audio visual (AV) PHY. Different PHYs are due to the demands of different applications, which were based on the development of the usage models for this standard. The SC PHY is designed to support low-cost and low-power mobile devices with low complexity. The HSI PHY is used for bidirectional, low-latency, non-line-of-sight high speed data transmission, such as an ad-hoc system to connect computers and devices around a conference table. The streaming of uncompressed video requires high throughput which is provided by the AV PHY. A minimum data rate is mandated by each PHY, and higher data rates are optional to best address the different market segments. In order to promote coexistence among these PHY modes, common mode signaling (CMS) with a low data rate of 25 Mb/s is defined to transmit/receive a synchronization frame in order to avoid interference between two or more operating devices.

Beamforming is supported by all the three PHY modes. A two-level mechanism is employed to find the optimum transmit and receive beams that enable high data rate transmission.

In the following discussions, SC PHY is the main focus because of its common use.

2.1.2 Frequency Allocation

IEEE 802.15.3c operates in the 60-GHz unlicensed band, from 57-66 GHz. A total bandwidth of 9 GHz is allocated, which is divided into four frequency channels with each channel bandwidth of 2.16 GHz, as shown in Fig. 2.1 and Table 2.1.

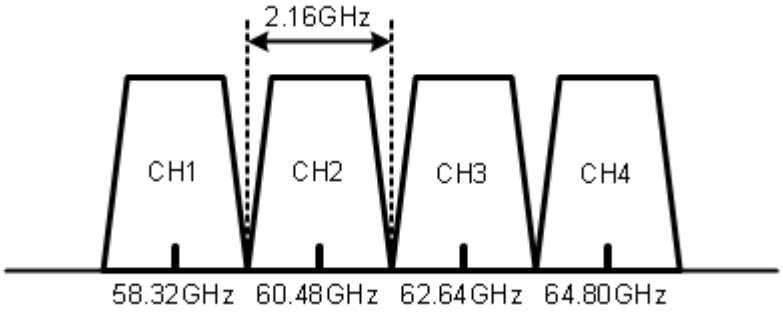

Fig. 2.1 Frequency allocation of IEEE 802.15.3c

Table 2.1 RF channelization of IEEE 802.15.3c

CHNL_ID	Start frequency	Center frequency	Stop frequency
1	57.24 GHz	58.32 GHz	59.40 GHz
2	59.40 GHz	60.48 GHz	61.56 GHz
3	61.56 GHz	62.64 GHz	63.72 GHz
4	63.72 GHz	64.80 GHz	65.88 GHz

2.1.3 Transmit Power

In different geographical regions, a compliant device should transmit a power with level not exceeding the power limit specified by appropriate regulatory bodies [2]. The power limit is summarized in Table. 2.2.

Table 2.2 Transmit power limit in different regions

Region	Maximum Transmit Power (dBm)	Maximum EIRP (dBm)	Maximum Antenna Gain (dBi)
USA/Canada	27	43.0	33.0 if P_{TX} = 10 dBm
Europe	13	57.0	30.0
Japan	10	58.0	47.0
Australia	10	51.8	41.8
Korea	10	27.0	17.0

2.1.4 Data Rate

Three classes of modulation and coding scheme (MCS) aiming for different wireless applications are provided by the single carrier mode specified in IEEE 802.15.3c. Class 1 is suitable for low-power low-cost mobiles with relatively high data rate of up to 1.5 Gb/s. Class 2 is able to achieve data rates up to 3 Gb/s. Class 3 features high performance with data rates exceeding 5 Gb/s.

The chip rate is constant at 1760 M chip/s corresponding to chip duration time of 0.568 ns. The data rates for different specified MCS classes are listed in Table 2.3.

Table 2.3 Date rates for different MCS classes in single carrier mode

MCS Class	Identifier	Data Rate (Mb/s)*	Modulation	Code Rate
Class 1	0	25.8	π/2 BPSK/(G)MSK	15/1024
	1	412		15/64
	2	825		15/32
	3	1650		15/16
	4	1320		3/4
	5	440		1/4
	6	880		1/2
Class 2	7	1760	π/2 QPSK	1/2
	8	2640		3/4
	9	3080		7/8
	10	3290		238/255
	11	3300		239/255
Class 3	12	3960	π/2 8-PSK	3/4
	13	5280	π/2 16-QAM	3/4

* With pilot word length = 0

2.1.5 Error Vector Magnitude

Error Vector Magnitude (EVM) is a measure of transmitter performance. For different classes of MCS in single carrier mode, it's specified and listed in Table 2.4.

Table 2.4 EVM for MCS classes in single carrier mode

MCS	EVM (dB)
Class 1	-7
Class 2	-14
Class 3	-21

2.1.6 Frame Error Rate

Frame error rate (FER) is a measure of the noise performance of the receiver. In single carrier mode, the frame error rate should be less than 8% with a frame payload length of 2048 octets in AWGN channel.

The probability of a frame received without error is expressed as:

$$(1-BER)^{2048\times 8} = 1-FER\ , \tag{2.1}$$

where BER is bit error rate. Therefore, BER is derived to be 5.09×10^{-6}.

2.1.7 Receiver Input Power

The minimum power level present at the input of the receiver for which the frame error rate is met is called the sensitivity. For different MCSs in single carrier mode, the reference sensitivity is listed in Table 2.5.

On the other hand, the maximum power level input to the receiver is also specified, and it should be at least -10dBm.

2.2 Link Budget

2.2.1 Radiated Power

In order to meet the requirement on power limit specified by appropriate regulatory bodies as show in Table 2.2, the transmitter is designed to transmit a maximum power of 10dBm. Assuming the antennas are in package with gain of 7dBi [3], the total radiated power is 17dBm.

Table 2.5 Receiver sensitivity for each MCS in single carrier mode

MCS identifier	Receiver Sensitivity (dBm)
0	-70
1	-61
2	-58
3	-55
4	-59
5	-65
6	-62
7	-58
8	-56
9	-54
10	-53
11	-52
12	-50
13	-46

2.2.2 Path Loss

Path loss (PL) is defined as the ratio of the output power of the transmit antenna to the input power available at the receive antenna. Basically, it's a function of the operating frequency. In free space, the path loss can be calculated by Friis Formula [4]:

$$PL = -20\log_{10}\left(\frac{\lambda}{4\pi R}\right), \tag{2.2}$$

where λ is the wavelength, R is the distance between the transmitter and the receiver.

For a 60-GHz signal with distance of 1 meter, the path loss in free space (PL_0) is 68dB. Therefore, the path loss at distance of R in practical channels can be calculated as:

$$PL = PL_0 + 10 \cdot n \cdot \log_{10} R \ , \tag{2.3}$$

where n is the channel parameter. For example, n is approximately to be 2 and 2.5 for simple line-of-sight (LOS) and non-line-of-sight (NLOS) channels, respectively.

2.2.3 E_b/N_0

Bit error rate (BER) is a function of E_b/N_0. The BER would typically decrease as E_b/N_0 increases in a certain channel. For different modulation and coding schemes in single carrier mode, the simulated results show the corresponding minimum required E_b/N_0 to meet the specified frame error rate with two mandatory usage models in residential environment. CM 1.3 and CM 2.3 are typical LOS and NLOS channel models, whose simulated BER performance are shown in Fig. 2.2 and Fig. 2.3 [5], respectively. Particularly, the MCS 13 in SC mode which offers the highest data rate requires minimum E_b/N_0 of 7.2 dB and 14.8 dB for CM 1.3 and CM 2.3 to achieve BER of 5.09×10^{-6}, respectively.

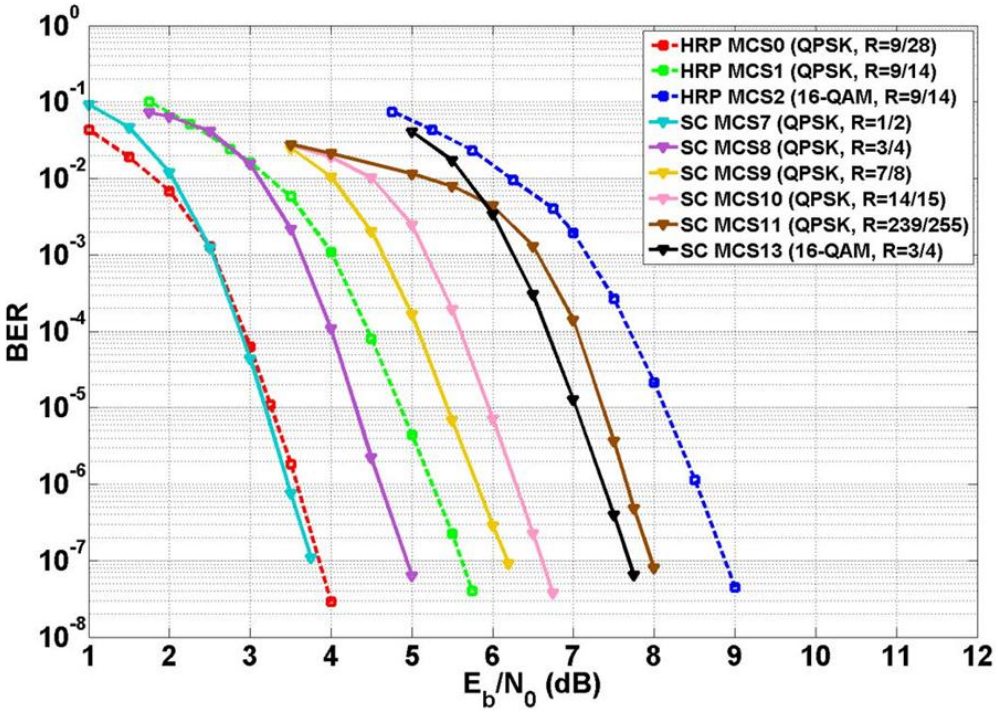

Fig. 2.2 BER performance of SC and OFDM PHY for CM1.3 (LOS)

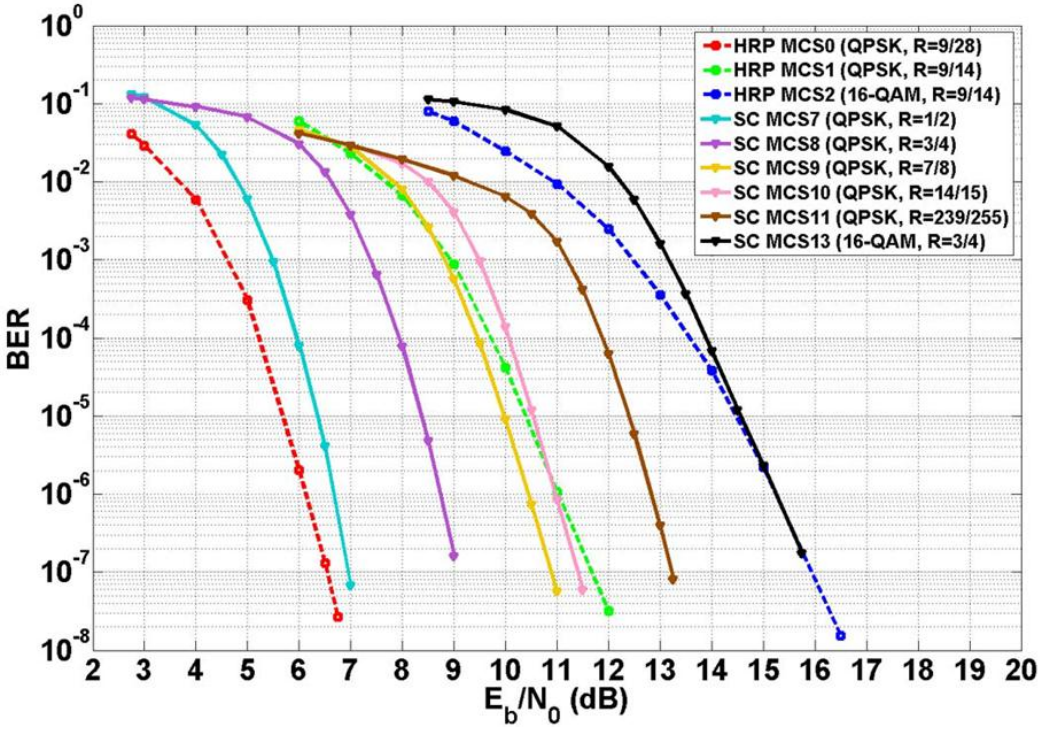

Fig. 2.3 BER performance of SC and OFDM PHY for CM2.3 (NLOS)

2.2.4 Tolerable Path Loss and Maximum Operating Range

The link budget corresponding to highest data rate in single carrier mode is calculated and summarized in Table 2.6. During calculation, it's assumed that both the transmit antenna and receive antenna have a gain of 7dBi [6] and the implementation loss is 6 dB, while the noise figure of the receiver is defined to be a typical value of 8dB [6]-[8].

For basic receiver, the tolerable path loss in NLOS channel is only 2.7dB, resulting operating range of 1.3m.

Fortunately, this very limited operating range can be improved by using phased-arrays. As discussed in next chapter, a 1×4 phased-array with 1 transmit elements and 4 receive elements can theoretically improve signal-to-noise ratio (SNR) by 6dB at the

receiver side [9]. As a result, the maximum operation range for NLOS channel is increased to be 3.5m.

Table 2.6 Link budget for single carrier mode of IEEE 802.15.3c

Parameter		LOS Channel	NLOS Channel
Bit Rate (R_b)		7.04 Gb/s	7.04 Gb/s
Power (P_{Tx})		10 dBm	10 dBm
Tx Antenna Gain (G_T)		7 dBi	7 dBi
Center Frequency (f_c)		60 GHz	60 GHz
Path Loss @ 1 m ($PL_0 = 20log_{10}(4\pi f_c/c)$)		68.00 dB	68.00 dB
Rx Antenna Gain (G_R)		7 dBi	7 dBi
Minimum E_b/N_0 (S)		7.2 dB	14.8 dB
Path Loss Exponent (n)		2.0	2.5
Implementation Loss (IL)		6 dB	6 dB
Rx Noise Figure Referred to the Antenna Terminal (NF)		8 dB	8 dB
Per Element	Average Noise Power Per Bit at Rx Input ($N = -174 + 10\ logR_b$)	-75.5 dBm	-75.5 dBm
	Average Noise Power Per Bit at Rx Output ($P_N = N+NF$)	-67.5 dBm	-67.5 dBm
	Tolerable Path Loss ($PL = P_{Tx}+G_T+G_R-P_N-S-IL-PL_0$)	10.3 dB	2.7 dB
	Maximum Operating Range ($d = 10^{PL/10n}$)	3.3 m	1.3 m
1×4 Phased-Array	Number of Tx Elements (N_T)	1	1
	Number of Rx Elements (N_R)	4	4
	Average Noise Power Per Bit at Rx Input ($N = -174 + 10\ logR_b + 10\ logN_R$)	-69.5 dBm	-69.5 dBm
	Average Noise Power Per Bit at Rx Output ($P_N=N_R+NF$)	-61.5 dBm	-61.5 dBm
	Tolerable Path Loss ($PL = P_{Tx}+G_T+20logN_T+G_R+20logN_R-P_N-S-IL-PL_0$)	21.4 dB	13.7 dB
	Maximum Operating Range ($d = 10^{PL/10n}$)	6.6 m	2.2 m

2.3 Receiver Specification

2.3.1 Conversion Gain

Conversion gain is a measure of the amplifying capability of a device and defined as the ratio of the output power (voltage) to the input power (voltage) where the input and output frequencies may be different. The cascaded conversion gain of a receiver is the sum of the voltage or power gain of each building block in the signal path.

The input voltage amplitude for an ADC with 1-V supply is assumed to be 0.25V, which is equal to -12dBV.

When operating at the lowest data rate of 25.8 Mb/s corresponding to MCS 0, the input power to the receiver is a minimum value of -70dBm which is equivalent to voltage swing of -80dBV for 50Ω impedance. Therefore, the maximum conversion gain is 68dB.

On the other hand, when the input power is maximum specified as -10dBm which is equivalent to voltage swing of -20dBV for 50Ω impedance, the conversion gain is minimum and derived to be 8dB.

As a result, the gain of the receiver has to be tunable from 8dB to 68dB to generate the same output power level to the ADC with different input power levels.

2.3.2 Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is an important parameter of a receiver and defined as the power ratio of the desired output signal to the noise, as shown below:

$$SNR = \frac{P_{in}}{N_{in}} = \frac{P_{in}}{N_o \cdot BW} \ , \tag{2.4}$$

where P_{in} is the input power, N_{in} is the input noise, N_o is spectral noise density, and BW is the bandwidth occupied.

In IEEE 802.15.3c standard, the required SNR is not directly specified. Instead, it should be derived from Eb/No together with modulation coding scheme.

E_b/N_o is expressed as:

$$\frac{E_b}{N_o} = \frac{P_{in}}{N_o} \cdot \frac{T_c}{n_c} \ , \tag{2.5}$$

where T_c and n_c are chip duration time and number of bits per chip, respectively.

From Eq. (2.4) and (2.5), the SNR is related to E_b/N_o, as shown below:

$$SNR = \frac{E_b}{N_o} \cdot \frac{1}{BW} \cdot \frac{n_c}{T_c} \ , \tag{2.6}$$

Since MCS 13 offers the highest data rate in SC PHY mode, it's targeted at and its requirement is calculated. In 2.2.3, E_b/N_o has been derived to be 7.2 dB and 14.8 dB for CM 1.3 and CM 2.3 to achieve required minimum BER. BW is specified to be 2.16 GHz for each of the four channels while T_c is equal to 0.568 ns. With π/2 16-QAM modulation, n_c of MCS 13 is 4. As a result, the required SNR is calculated to be 12.3dB and 19.9dB for LOS channel model CM 1.3 and NLOS channel mode CM 2.3, respectively.

2.3.3 Noise Figure

Noise factor is a measure of the noise performance of a receiver and defined as the ratio of input SNR to output SNR. When expressed in dB scale, it's named noise figure (NF).

$$\begin{aligned} NF &= P_{in} - N_{in} - SNR_{out} \\ &= P_{in} - N_o - 10\log BW - SNR_{out} \\ &= P_{in} - 10\log BW - SNR_{out} + 174 \end{aligned} \quad , \tag{2.7}$$

For MCS 13, the minimum P_{in} is defined by the sensitivity which is -46dBm. Therefore, the noise figure is calculated as follows:

$$NF = -46 - 10\log(2.16G) - 19.9 + 174 = 14.8(dB) \quad , \tag{2.8}$$

To have better SNR which may be required by future more complicated channel model or higher data rate or longer operation distance, the targeted noise figure of the receiver is 8dB, which is close to the state-of-the-art value.

The cascaded noise figure of a receiver [10] is dominated by the noise figure and gain of the LNA. The contribution from the following stages diminishes thanks to the positive gain introduced by the previous stages.

2.3.4 Linearity

Commonly used parameters to characterize the linearity of a receiver are 1-dB compression point (P_{1dB}) and input referred third-order interception point (IIP3). P_{1dB} defines the input power level at which the amplifier's gain is 1dB less than the small signal gain, or is compressed by 1dB. IIP3 defines the input power level at which the output third-order product intercepts with the output fundamental tone.

In IEEE 802.15.3c standard, the maximum input power to the receiver is specified to be -10dBm, so P_{1dB} is chosen to be -10dBm.

However, when there are interferers located at adjacent channels, their intermodulation product may reduce the SNR and even completely corrupt the desired received signal, as shown in Fig. 2.4.

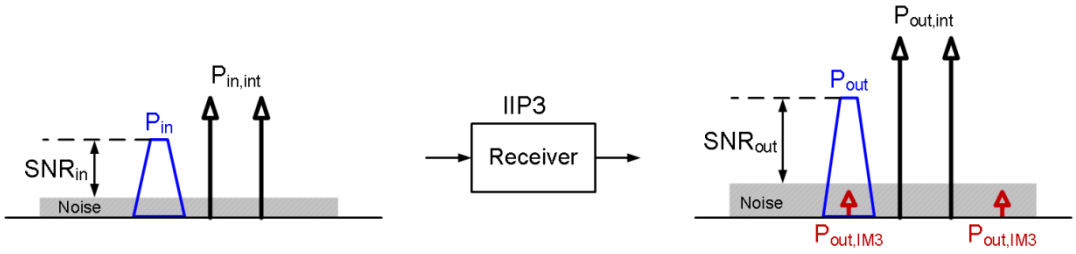

Fig. 2.4 Intermodulation product generated by interference signals

The third-order intermodulation product $P_{out,\ IM3}$ is related to IIP3 [10], as show below:

$$\frac{P_{out,\text{int}}}{P_{out,IM3}} = \left(\frac{IIP3}{P_{in,\text{int}}} \right)^2 . \tag{2.9}$$

The gain is the same for both desired signal and interference, so it's written as:

$$\frac{P_{out,\text{int}}}{P_{in,\text{int}}} = \frac{P_{out}}{P_{in}} . \tag{2.10}$$

From Eq. (2.9) and (2.10), the third-order intermodulation product is derived as to be:

$$\frac{P_{out,IM3}}{P_{out}} = \frac{P_{in,\text{int}}^3}{P_{in} \cdot IIP3^2} . \tag{2.11}$$

In order to obtain the required SNR, the intermodulation product should be lower than the noise level when the power of desired input signal is the minimum. Therefore, Eq. (2.11) is rewritten as:

$$\frac{P_{out,IM3}}{P_{out}} = \frac{P_{in,\text{int}}^3}{P_{in} \cdot IIP3^2} \le \frac{N_{out}}{P_{out}} = \frac{1}{SNR_{out}} \quad . \tag{2.12}$$

As such, the requirement on IIP is derived:

$$IIP3 \ge \sqrt{\frac{P_{in,\text{int}}^3}{P_{in}} \cdot SNR_{out}} \quad , \tag{2.13}$$

which can be rewritten in dB scale as:

$$IIP3 \ge P_{in,\text{int}} + \frac{P_{in,\text{int}} - P_{in} + SNR_{out}}{2} \quad . \tag{2.14}$$

For MCS 13, the minimum input power is -46dBm and the minimum SNR_{out} is 19.9dB for CM 2.3 channel model. Assuming that the interference signal comes from a transmitter located in 10cm away with transmit power of 10dBm and an antenna gain of 7dBi, the received signal by the receive antenna with 7dBi gain is calculated as:

$$P_{\text{int}erference} = P_{TX} + G_T - PL_{@1cm} + G_R = 10 + 7 - 48 + 7 = -24 \ \left(dBm\right) \quad . \tag{2.15}$$

Therefore, the corresponding required IIP3 is derived to be -3dBm.

For a 4×4 phased-array transceiver, the interference is 12dB larger due to spatial power combining. Fortunately, its beamforming nature can help to reduce the interference by properly rotating the beam direction. For example, a phased-array with peak-to-null ratio of 25dB can ideally reduce the power received interference to be -37dBm. As a result, the required IIP3 is ideally relaxed to be -22dBm.

2.3.5 Specification Summary

Similar to the above steps, specification for more cases such as different MCS classes in SC mode and different input power levels are calculated and derived. Finally, the detailed specification is summarized in Table 2.7.

Table 2.7 Specification of receiver RF font-end

Parameters	**IEEE 802.15.3c**	**Specification**
Frequency [GHz]	57 ~ 66	57 ~ 66
Voltage Gain[dB]	8 (low gain) 68 (high gain)	8 (low gain) 74 (high gain)
Noise Figure [dB]	50.0 (low gain) 14.0 (high gain)	44.0 (gain=8) 8.0 (gain=74~50)
IIP3 [dBm]	--	-3 (gain=8)
P_{1dB} [dBm]	-10	-10
Sensitivity [dBm]	-70 for MCS0 -58 for MCS7 -46 for MCS13	-76 for MCS0 -64 for MCS7 -52 for MCS13
Input Matching S11 [dB]	--	-10

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Chapter 3

Phased-Array Receiver Architecture

3.1 Overview of Receiver Architectures [1]

To implement 60-GHz receiver, the existing system architectures have to be studied carefully to know the trade-offs and thus choose the optimal architecture. Moreover, basic architectures are the foundations to construct phased-array systems. In this subsection, some commonly used receiver architectures are investigated, including super heterodyne topology, direct-conversion topology and dual-conversion zero-IF topology.

3.1.1 Super Heterodyne Topology

A super heterodyne receiver is shown in Fig. 3.1. The RF signal is amplified and down-converted to IF, whose frequency is much lower than the RF frequency. As such, the channel selection filter (CSF) is with reasonable quality factor and realizable. Super heterodyne topology features several advantages. LO leakage to the antenna and LO pulling by the power amplifier are typically trivial as long as LO frequency is quite different from the RF frequency. The DC offset due to LO leakage and hence LO self-mixing don’t affect the IF.

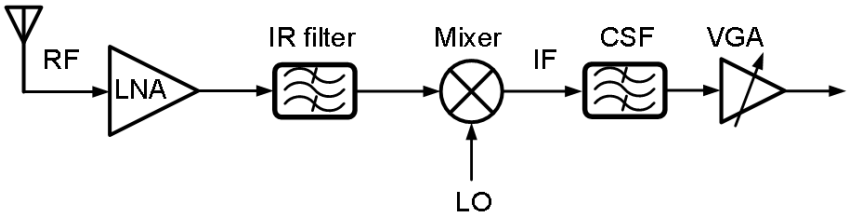

Fig. 3.1 A super heterodyne receiver

However, the image signal is also down-converted and the IF signal may be corrupted. Therefore, an image-rejection filter (IR filter) is necessary to sufficiently suppress the unwanted harmful image signal. Moreover, the baseband operates at IF frequency and thus high power consumption is expected. In targeted IEEE 802.15.3c standard, the signal bandwidth is already 2.16GHz that any additional IF frequency would significantly increase the power consumption of the ADC.

3.1.2 Direct-Conversion Topology

The direct-conversion architecture is shown in Fig. 3.2. The LO frequency is the same as RF frequency and thus the IF frequency is at DC. As long as there is no image signal, image rejection filter is eliminated. Besides, a simple low-pass filter can be used for channel selection.

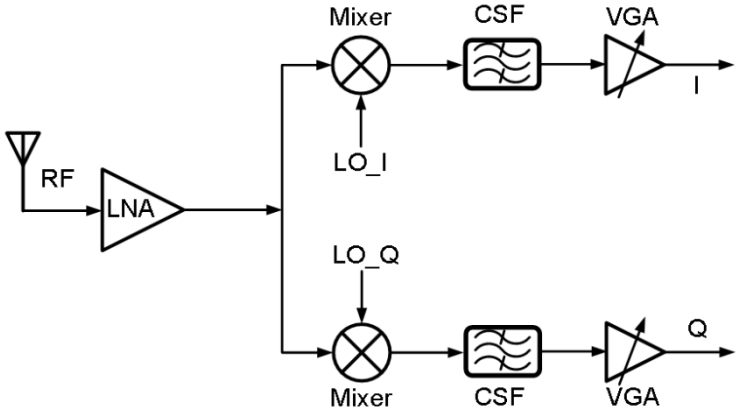

Fig. 3. 2 A direct-conversion receiver

However, to avoid information loss due to positive and negative spectrum overlapping, quadrature paths should be employed and accurate I/Q phases are required for the LO. Unlike super-heterodyne topology, a direct-conversion receiver suffers from LO leakage, LO pulling and LO self-mixing induced DC offsets, because the LO frequency is the same as RF frequency. DC offsets generated in the mixer due to mismatches are amplified and would saturate the following stages, including the CSF, VGA and ADC.

3.1.3 Dual-Conversion Zero-IF Topology

In this architecture, two frequency conversions are utilized, as shown in Fig. 3.3. The RF signal is first down-converted to an IF1 frequency and then down-converted by a second mixer. The resultant IF frequency is located at zero. To avoid information loss which is the same scenario as direct-conversion, quadrature paths are necessary. It needs no image-rejection filter, since the IF1 is relatively high that the image signal is very far from the desired signal and thus can be easily filtered out by the band-pass filtering characteristic of the LNA. Frequency pulling, LO leakage and self-mixing is not important because the frequencies of RF, first LO and second LO are totally different. Although more components are needed than direct-conversion architecture, smaller power consumption is possible because of the lower frequency they are operating at. Besides, by properly locating the frequencies, the LOs required can be generated with one frequency synthesizer.

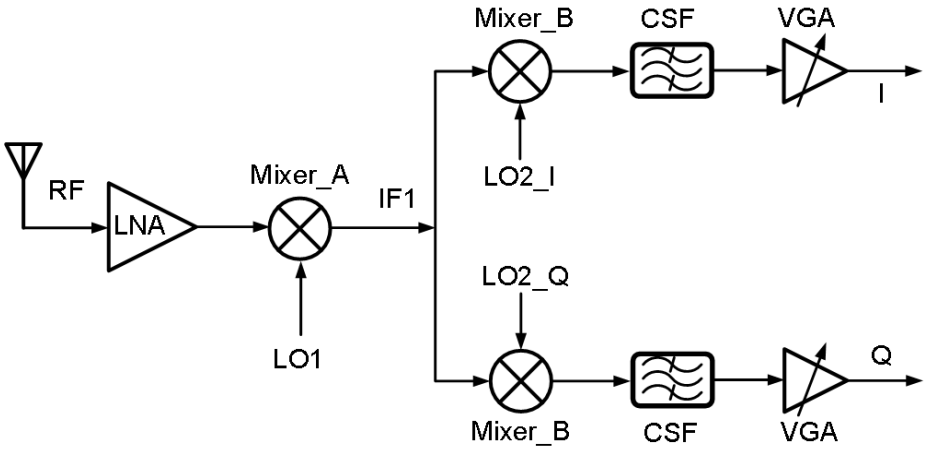

Fig. 3.3 A dual-conversion zero-IF receiver

3.1.4 Summary on Receiver Topology for IEEE 802.15.3c

The channel bandwidth of IEEE 802.15.3c is 2.16 GHz. Therefore, super heterodyne architecture is not suitable due to the need of ultra-high-speed ADC. The operation frequency of ADC can be relaxed by using I/Q paths with two ADCs. As such, direction-conversion or dual-conversion zero-IF architectures are widely used in literatures [2]-[3].

3.2 Phased-Array Receiver Architectures

Phased-arrays are a special class of multiple antenna systems that exhibit spatial power combining and electronic beamforming by time delay compensation in the signal paths of different elements [4]. Phased-arrays have played a key role in boosting signal quality through spatial diversity, interference mitigation via spatial filtering, and data rates with spatial multiplexing. [5]

3.2.1 Phased-Array Principles [5]-[6]

An N-element simple antenna array with antenna distance of d is shown in Fig. 3.4. A plane wave impinges on each element at an angle θ relative to the array normal. The signal at the Element k is then given by:

$$x_k(t) = \mathrm{Re}\left[\tilde{x}_1(t-k\Delta_0)\exp\left(j2\pi f_c(t-k\Delta_0)\right)\right], \tag{3.1}$$

where Δ_0 is the relative time of flight between two adjacent elements and expressed as:

$$\Delta_0 = d\sin\theta / c \ . \tag{3.2}$$

θ is the incident angle and c is the propagation velocity.

For a narrowband signal with bandwidth much smaller than the carrier frequency, the array output for the system in Fig. 3.4 can be written as:

$$\begin{aligned} y(t) &= \mathrm{Re}\left\{\sum_{k=0}^{N-1}\tilde{x}_1(t-k\Delta_0)\exp\left[j2\pi f_c(t-k\Delta_0)\right]\right\} \\ &\approx \mathrm{Re}\left\{\left[\sum_{k=0}^{N-1}\exp\left(-j2\pi f_c k\Delta_0\right)\right]\tilde{x}_1(t)\exp\left(j2\pi f_c t\right)\right\} \end{aligned} . \tag{3.3}$$

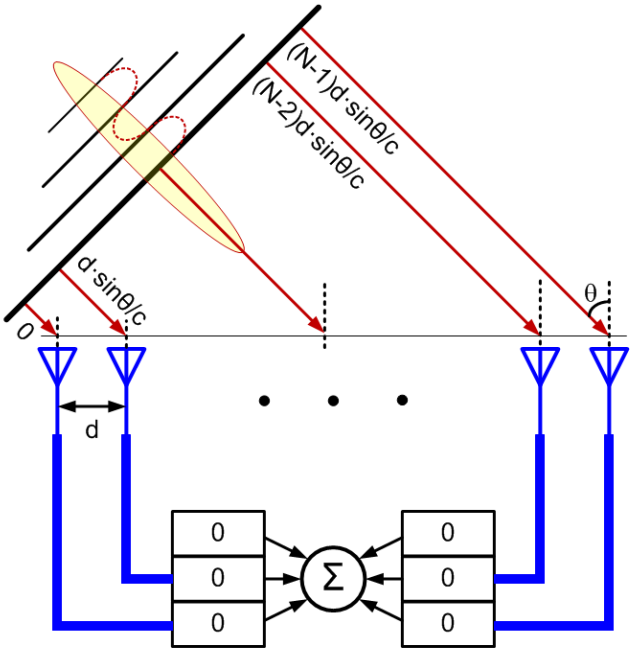

Fig. 3.4 A simple receiver array

By defining ψ as:

$$\psi = 2\pi f_c \Delta_0 \ , \tag{3.4}$$

which can be interpreted as equivalent to an "electrical envelope phase shift" for each element, the complex envelope of the array output is derived as:

$$\tilde{y}(t) = \left[\sum_{k=0}^{N-1} \exp\left[-jk\psi\right]\right] \tilde{x}_1(t) \ . \tag{3.5}$$

As a result, the array gain is derived to be:

$$G(\psi) = \left[\sum_{k=0}^{N-1} \exp\left(-jk\psi\right)\right] = e^{-\frac{j(N-1)\psi}{2}} \frac{\sin\left(\frac{N\psi}{2}\right)}{\sin\left(\frac{\psi}{2}\right)} \ . \tag{3.6}$$

As shown in Fig. 2.5, if variable phase shifts are introduced, the signal received by each element is electrically phase shifted by an angle φ relative to its neighboring element. Therefore, the array output can be expressed as:

$$\tilde{y}(t) = \left[\sum_{k=0}^{N-1} \exp\left[-jk\left(\psi+\varphi\right)\right]\right] \tilde{x}_1(t) = A\left(\psi+\varphi\right)\cdot \tilde{x}_1(t) \ . \tag{3.7}$$

Accordingly, the array gain is derived to be:

$$G(\psi) = \left[\sum_{k=0}^{N-1} \exp\left(-jk\left(\psi+\varphi\right)\right)\right] = e^{-\frac{j(N-1)\psi}{2}} \frac{\sin\left(\frac{N\left(\psi+\varphi\right)}{2}\right)}{\sin\left(\frac{\left(\psi+\varphi\right)}{2}\right)} \ . \tag{3.8}$$

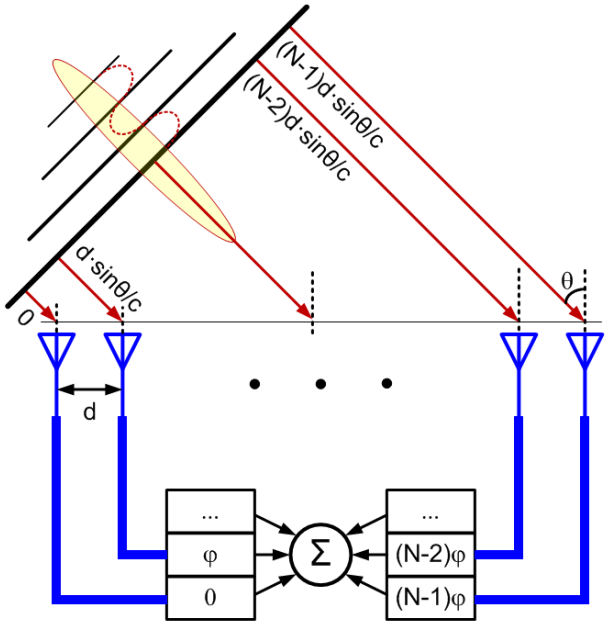

Fig. 3.5 A phased-array receiver

Clearly, the beam direction is rotated by an angle of φ, which is equivalent to a spatial angle of:

$$\theta_0 = \sin^{-1}\left[-(\varphi/2\pi)(\lambda/d)\right] \quad . \tag{3.9}$$

Therefore, the array gain now has a peak in the direction of the angle θ_0.

If the spacing d is too large compared to a wavelength, the array pattern will have a grating lobe, which happens at an angle of θ_0' expressed as:

$$\frac{2\pi}{\lambda} d \sin\theta_0' - \varphi = \pm 2\pi \quad . \tag{3.10}$$

From Eq. (3.9) and (3.10), it can be derived that:

$$\sin\theta_0' = \sin\theta_0 \pm \frac{\lambda}{d} \quad . \tag{3.11}$$

To prevent a grating lobe, the following condition should be satisfied:

$$\frac{d}{\lambda} \le \frac{1}{1+\left|\sin\theta_0\right|} \quad , \tag{3.12}$$

which indicates that the spacing d should not be larger than half of the wavelength. As such, the elements are so close to each other that the received signals are tightly correlated in amplitude. Thus, the signals add in amplitude while any uncorrelated noise signals add in power. Consequently, SNR gets improved by $10\log_{10}N$ as the element number N increases.

On the transmit side, the output power gets increased by $20\log_{10}N$ due to special power combining. Overall, an N×N phased-array with N transmit elements and N receive element improves the link budget by $30\log_{10}N$.

3.2.2 Phase Shifting Configurations

To steer the beam direction of a phased-array receiver, phase shifters can be implemented in different stages: RF, LO, IF or digital baseband [7]-[8].

3.2.2.1 RF Phase Shifting

In RF phase shifting architecture [2]-[3], the RF signals get phase shifted and combined at RF, and further down-converted to IF or baseband, as shown in Fig. 3.6.

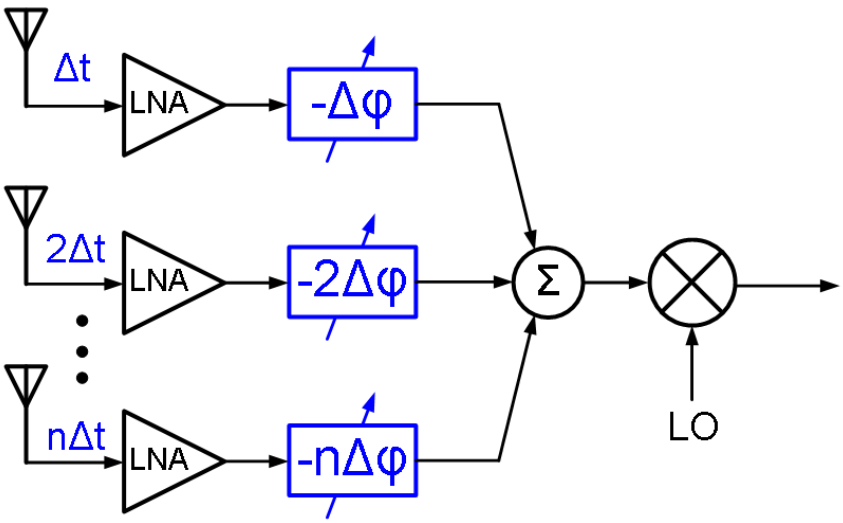

Fig. 3.6 RF phase shifting configuration

There is only one down-conversion path, including mixers, analog and digital baseband. Moreover, the unwanted signals are suppressed before going to the mixers, so that the dynamic range requirement of the mixers is relaxed. However, the performance of the phase shifters in terms of loss, noise figure, linearity and mismatches directly affects the system since the phase shifters are in signal path, let alone with high frequency and process variation taken into account. Particularly, the phase shifter should have sufficient dynamic range to tolerate the signal level fluctuations.

3.2.2.2 LO Phase Shifting

In LO phase shifting, the LO signals are phase shifted [7, 9], as shown in Fig. 3.7.

The main advantage over RF phase shifting is that the system performance is not sensitive to the performance of phase shifter. Therefore, the requirement of the phase shifter in terms of noise figure, linearity, loss and amplitude mismatches gets much relaxed. However, more mixers are needed as compared with RF phase shifting, and those mixers should have high dynamic range to tolerate the interference signals. Besides, the large LO signals must be routed and distributed to different paths, introducing issues such as cross-talk and phase coherence.

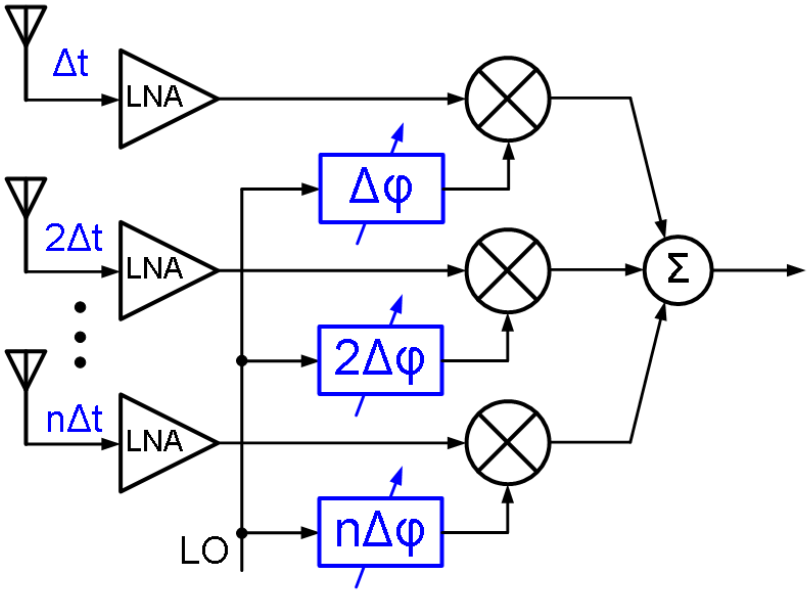

Fig. 3.7 LO phase shifting configuration

3.2.2.3 IF Phase Shifting

Phase shift can be implemented in the IF path, as shown in Fig. 3.8.

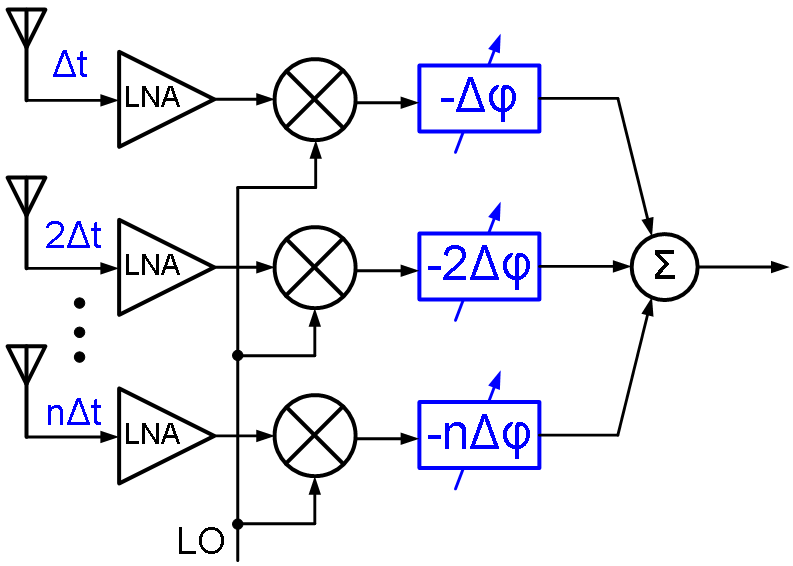

Fig. 3.8 IF phase shifting configuration

However, this approach also requires multiple mixers and still suffers from the system performance degradation due to the phase shifter appearing in signal paths. This architecture is not a proper option for low cost and low power phased-array [3].

3.2.2.4 Digital Phase Shifting

The phase shifting can be implemented in digital baseband, as shown in Fig. 3.9.

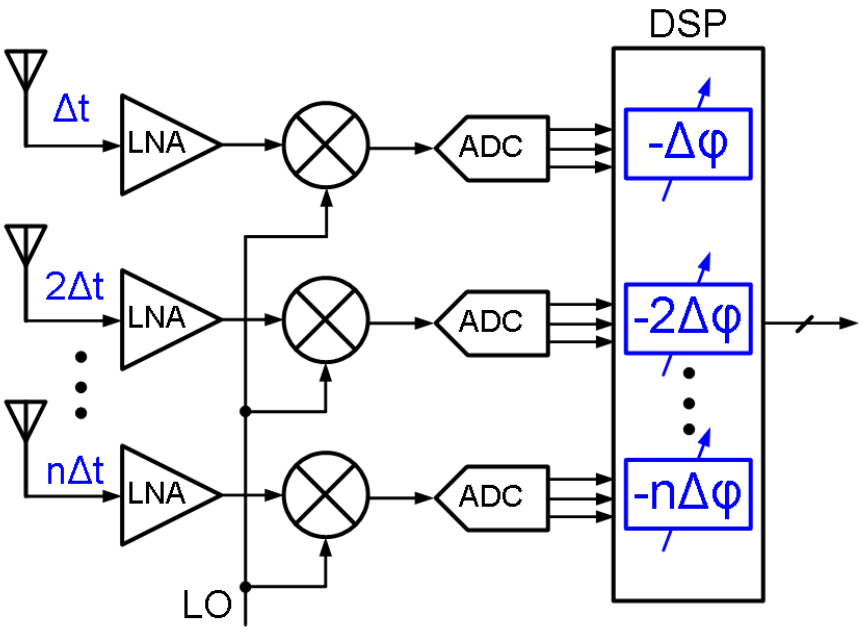

Fig. 3.9 Baseband phase shifting configuration

This configuration features high flexibility and high phase shift accuracy while no dedicated hardware for phase shifters is needed. Concurrent independent multiple beams are allowed. However, multiple mixers and high speed ADCs are required, so substantial complexity and high power consumption are resulted in.

3.2.2.5 Summary on Phase Shifting Configuration

The phase shifting configuration should be designed carefully according to the requirement of applications. RF phase shifting requires the least number of hardware but suffers from system performance degradation. It's more proper to be used to implement phased-array with a large number of elements, since the complexity is a main concern while the performance degradation could be compensated by more elements. LO phase shifting is popular when the element number is small, which is

typically not more than 8. Digital domain phase shifting offers the unique capability of concurrent beams. IF phase shifting has comparable complexity with LO phase shifting but the system performance is very sensitive to the phase shifter.

3.2.3 Phased-Array Architectures

From the above discussions, the phased-array architecture is more proper to be based on direct-conversion topology or dual-conversion zero-IF topology.

3.2.3.1 Direct-Conversion with LO Phase Shifting

A 4-path phased-array receiver based on direct-conversion architecture with LO phase shifting configuration is shown in Fig. 3.10.

8 mixers, 8 phase shifters and 8 LO distribution trees are required. Both the LO and the phase shifters operate at 60 GHz, and thus they are power hungry and area consuming. In addition, routing multiple 60-GHz signals with different phases is quite challenging.

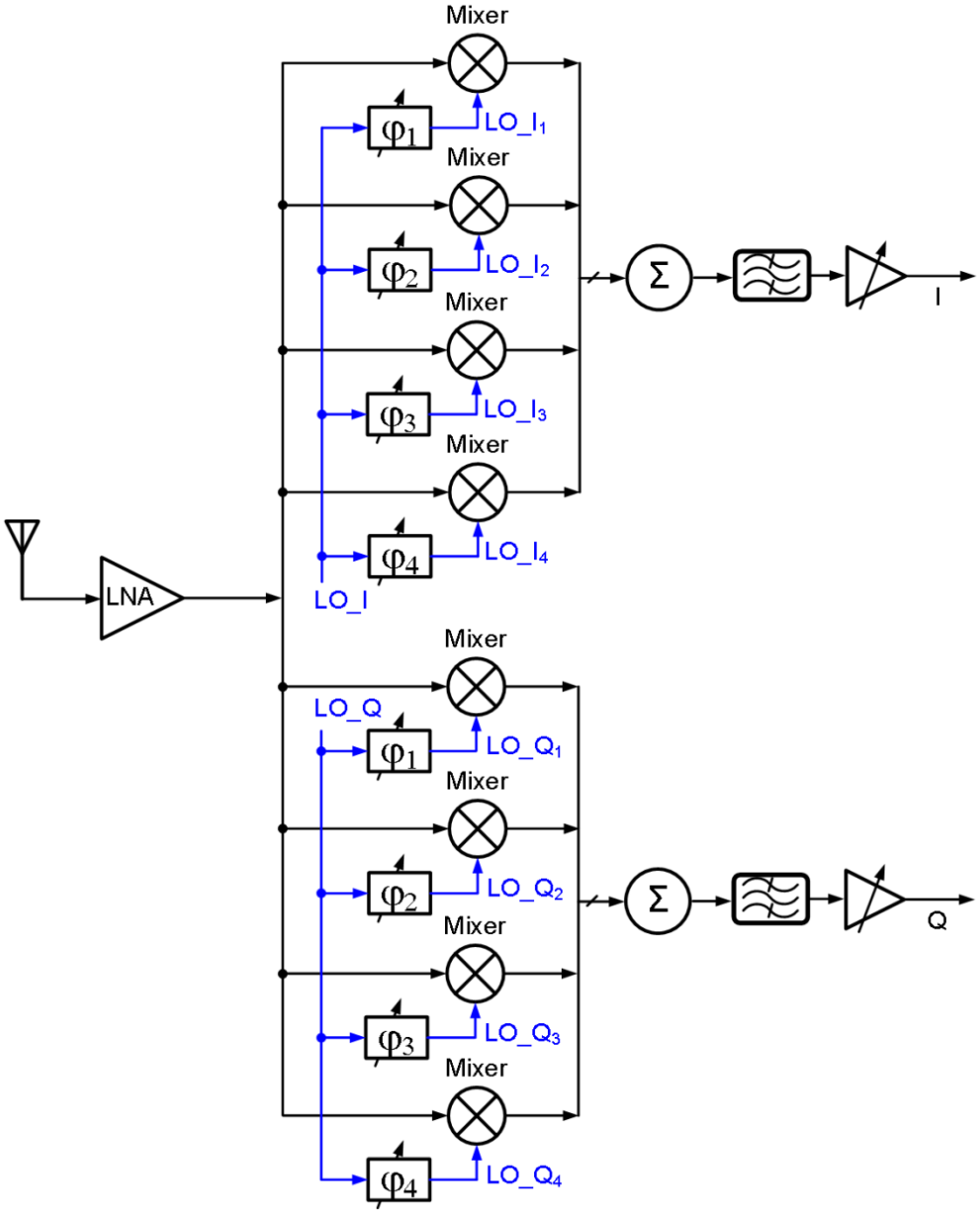

Fig. 3.10 4-path phased-array with direct-conversion and LO phase shifting

3.2.3.1 Dual-Conversion Zero-IF with LO Phase Shifting

A 4-path phased-array receiver based on dual-conversion zero-IF architecture with LO phase shifting configuration is shown in Fig. 3.11.

Obviously, compared with direct-conversion, the components needed are less and they are working at lower frequencies. Therefore, dual-conversion zero-IF architecture is more suitable to be employed for the 4-path phased-array receiver.

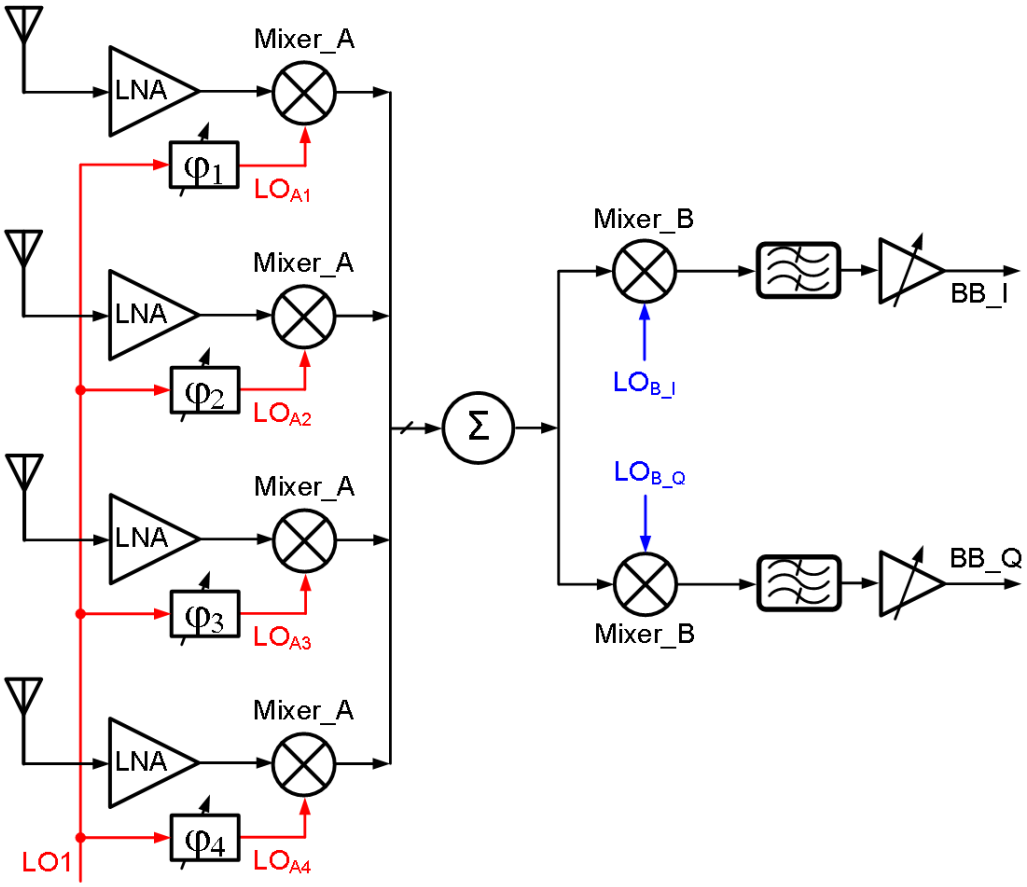

Fig. 3.11 4-path phased-array with dual-conversion zero-IF and LO phase shifting

3.3 Proposed 4-Path Phased-Array Receiver RF Front-End

3.3.1 Number of Paths

An N-path phased-array receiver improves the link budget by $10\log_{10}N$. Targeted at IEEE 802.15.3c, Table 3.1 and Fig. 3.12 show the corresponding operation range at NLOS channel for different path number N.

Table 3.1 Operation range for different path number

Path No.	Max. Operation Range (m)
1	1.28
2	1.70
3	1.99
4	2.24
5	2.45
6	2.63
7	2.80
8	2.95
9	3.09
10	3.23
11	3.35
12	3.47
13	3.58
14	3.69
15	3.80
16	3.89

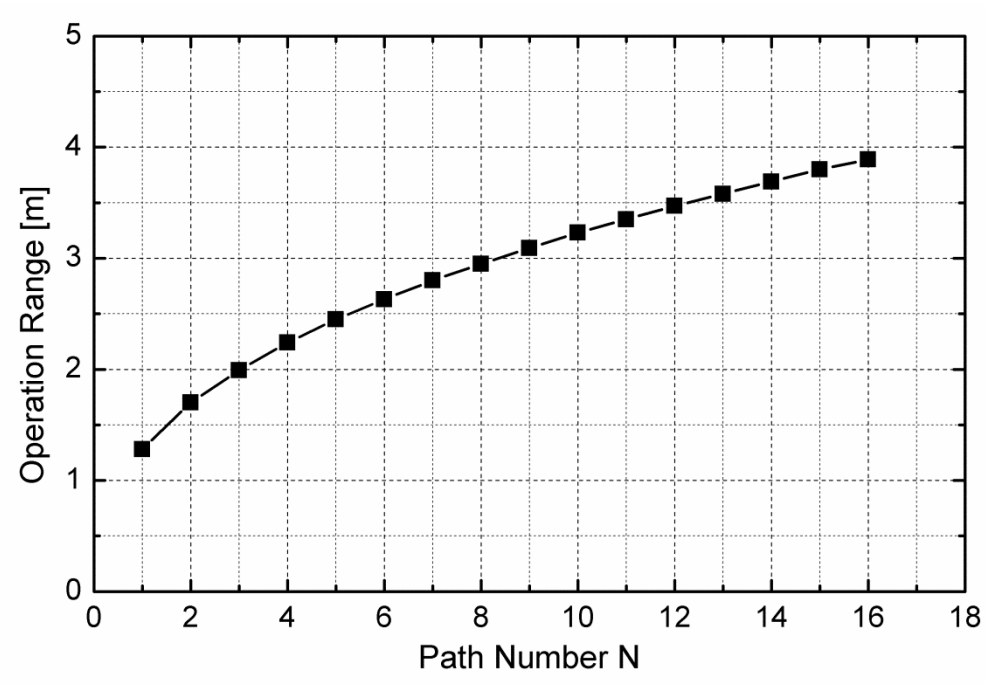

Fig. 3.12 Maximum operation range for different path number

For short-range applications such as wireless links to replace desktop cables, the communication distance is generally within 1.5 meters and thus path number of 2 is enough theoretically. To have some margins for real application, path number of 4 is an optimal choice. Using a larger number could increase the communication distance, but the operation range tends to increase less and less with N. For example, 2.24-m operation range requires path number of 4 but 3.89-m requires path number of 16. In practice, the efficiency of each path would degrade due to the complicated long signal routing and coupling. At the same time, the chipset cost becomes much higher due to larger chip area and hence lower yield. As a result, path number of 4 is chosen for the phased-array receiver system.

3.3.2 System Architecture

As shown in Fig. 3.13, the proposed phased-array receiver RF font-end is based on dual-conversion zero-IF topology. Each element has its own first down-conversion, while the second down-conversion stages are shared by two neighboring elements thus only two IF I/Q paths are required. By doing so, the array pattern can be reconfigured to produce either two independent beams concurrently, each by two-element groups, or one single beam by all four elements, depending on the link budget requirement of applications.

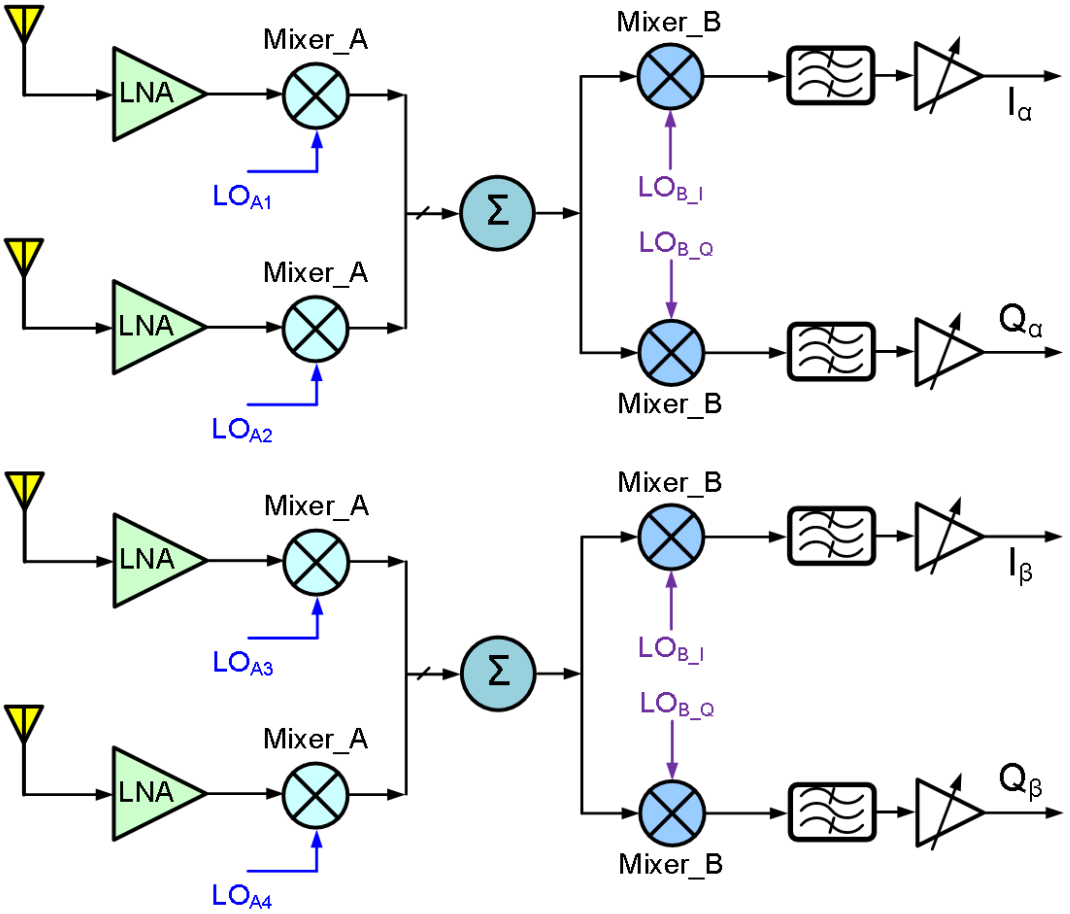

Fig. 3.13 Proposed phased-array receiver RF front-end

The frequency synthesizer needs to generate two LO outputs with the second LO having both in-phase and quadrature-phase outputs. Normally, the frequency of the second LO is designed to be an integer fraction of the first LO frequency. Assuming the frequency ratio is 1/n, the frequency relation between RF, the first LO and the second LO can be written as:

$$f_{RF} = f_{LO_A} + f_{LO_B} = \left(1 + \frac{1}{n}\right) f_{LO_A} \quad . \tag{3.13}$$

For different n, the corresponding LO frequencies are listed in Table 3.2, assuming the RF frequency is at 60 GHz. If n is 1, the LOs have the same frequency, which is desired for the frequency generation. However, the leakage of the first LO to the signal

path would mix with the second LO and thus may corrupt the desired RF signal. A new architecture with 30-GHz LO was proposed in [10], but poly-phase filter is required in signal path which is typically not good. For n larger than 3, the frequency of the first LO is high and the division/multiplication ratio is too large to implement easily. Compared with n=2, n=3 features lower IF1 frequency and thus the IF1 routing and power combining would be less challenging. Therefore, n is designed to be 3.

Table 3.2 LO frequencies for different frequency ratios

Frequency Ratio n	f_{LOA} (GHz)	f_{LOB} (GHz)
1	30	30
2	40	20
3	45	15
4	48	12
5	50	10

3.3.3 Specification of 4-Path Phased-Array Receiver

To meet the receiver specification in Section 2.3.5, the parameters of target 4-path phased-array receiver are derived and summarized in Table 3.3.

Table 3.3 Specification of 4-path phased-array receiver

Parameters		IEEE 802.15.3c	Specification
Frequency [GHz]		57 ~ 66	57 ~ 66
Element	Voltage Gain [dB]	-4 (low gain) 56 (high gain)	-4 (low gain) 62 (high gain)
	Noise Figure [dB]	50.0 (low gain) 14.0 (high gain)	44.0 (gain=-4) 8.0 (gain=62~38)
	IIP3 [dBm]	--	-22
	P_{1dB} [dBm]	-10 (low gain)	-10 (low gain)
	Sensitivity [dBm]	-64 for MCS0 -52 for MCS7 -40 for MCS13	-70 for MCS0 -58 for MCS7 -46 for MCS13
	Input Matching S11 [dB]	--	-10
	Power Per Element [mW]	--	50 @1.2V
Phased-Array	Element Number	--	4
	Voltage Gain[dB]	8 (low gain) 68 (high gain)	8 (low gain) 74 (high gain)
	IIP3 [dBm]	--	-3
	P_{1dB}[dBm]	-10 (low gain)	-10 (low gain)
	Sensitivity [dBm]	-70 for MCS0 -58 for MCS7 -46 for MCS13	-76 for MCS0 -64 for MCS7 -52 for MCS13
	Total Power [mW]	--	RF: 200 @1.2V LO: 80 @1.0V
	Phase Control	--	360° 4 bits
	Peak-to-Null Ratio [dB]		25
	Technology	--	65nm CMOS

3.3.4 Specification of Building Blocks

The building blocks design in the receiver chain has to consider many trade-offs in terms of noise figure, gain, linearity and power consumption. For example, the overall receiver gain can be distributed over different stages. The large gain at the first stage is desired to relax the NF requirement for the following stages but the linearity would be sacrificed.

When the input power is large that SNR is sufficient, linearity is the main concern. So the LNA is allowed to have lower gain and thus to obtain higher linearity though the NF may be high. On the other hand, when the input power is small, SNR is important while linearity is typically trivial, and thus LNA should have high gain and low NF. Therefore, LNA with variable gain is desired to make trade-offs between NF and linearity depending on different input power levels.

3.3.4.1 LNA

Since the LNA dominates the system NF of the receiver, NF of less than 8 dB (including the loss of the off-chip single-end-to-differential balun and input matching network) is needed. On one hand, LNA is required to provide 20-dB gain to suppress the NF contribution from later stages. On the other hand, to relax the linearity requirement of the coming building blocks, a reduced gain (-12 dB) is preferred at maximum received power situation. The specification of LNA is shown in Table 3.4.

Table 3.4 Specification of LNA

Parameters	Specifications
Frequency (GHz)	CH1: 57.24~59.40 CH2: 59.40~61.56 CH3: 61.56~63.72 CH4: 63.72~65.88
Voltage Gain (dB)	-12 ~ 20
Noise Figure (dB)	≤ 7.0 (high gain)
IP_{1dB} (dBm)	-8 (low gain)
Input Matching S11 (dB)	≤ -10
Current Consumption (mA)	35
Supply Voltage (V)	1.2

3.3.4.2 Mixer A

As long as the NF contribution from Mixer A can be mostly suppressed by LNA, the NF is relaxed to be 16dB. A gain of 3dB would help further reduce the noise contribution from the later stages. The specification of first down-conversion mixer (Mixer A) is shown in Table 3.5.

Table 3.5 Specification of Mixer A

Parameters	Specifications
RF Frequency (GHz)	CH1: 57.24~59.40 CH2: 59.40~61.56 CH3: 61.56~63.72 CH4: 63.72~65.88
LO Frequency (GHz)	CH1: 43.74 CH2: 45.36 CH3: 46.98 CH4: 48.60
IF1 Frequency (GHz)	CH1: 13.50~15.66 CH2: 14.04~16.20 CH3: 14.58~16.74 CH4: 15.12~17.28
Voltage Gain (dB)	3
Noise Figure (dB)	16
IP_{1dB} (dBV)	-20
Current Consumption (mA)	10
Supply Voltage (V)	1.2

3.3.4.3 Mixer B

The specification of first down-conversion mixer (Mixer B) is shown in Table 3.6.

Table 3.6 Specification of Mixer B

Parameters	Specifications
RF Frequency (GHz)	CH1: 13.50~15.66 CH2: 14.04~16.20 CH3: 14.58~16.74 CH4: 15.12~17.28
LO Frequency (GHz)	CH1: 14.58 CH2: 15.12 CH3: 15.66 CH4: 16.20
IF1 Frequency (GHz)	0 ~ 1.08
Voltage Gain (dB)	-2
Noise Figure (dB)	16
IP_{1dB} (dBV)	-17
Current Consumption (mA)	10
Supply Voltage (V)	1.2

3.3.4.4 First LO

The specification of the LO for first down-conversion is shown in Table 3.7.

Table 3.7 Specification of the first LO (LO_A)

Parameters	Specifications
Frequency (GHz)	43.74 ~ 48.6
Phase Noise (dBc@1MHz offset)	-98
Supply Voltage (V)	1.2

3.3.4.5 Second LO

The specification of the LO for second down-conversion is shown in Table 3.8.

Table 3.8 Specification of the second LO (LO_B)

Parameters	Specifications
Frequency (GHz)	14.58 ~ 16.20
Phase Noise (dBc@1MHz offset)	-108
I/Q Phase Error ( )	< 2.0
I/Q Amplitude Error (dB)	< 1.0
Supply Voltage (V)	1.2

3.3.4.6 Phase Shifter

The specification of the phase shifter is shown in Table 3.9.

Table 3.9 Specification of the phase shifter

Parameters	Specifications
Output Frequency (GHz)	42.75 ~ 49.5
Phase Resolution ( )	22.5
Phase Error ( )	< 2.0
Amplitude Variation (dB)	< 1.5
Supply Voltage (V)	1.2

3.3.5 Behavioral System Simulation

To verify the specification of each building block, behavioral simulation on system level is performed in ADS, as shown in Fig. 3.14.

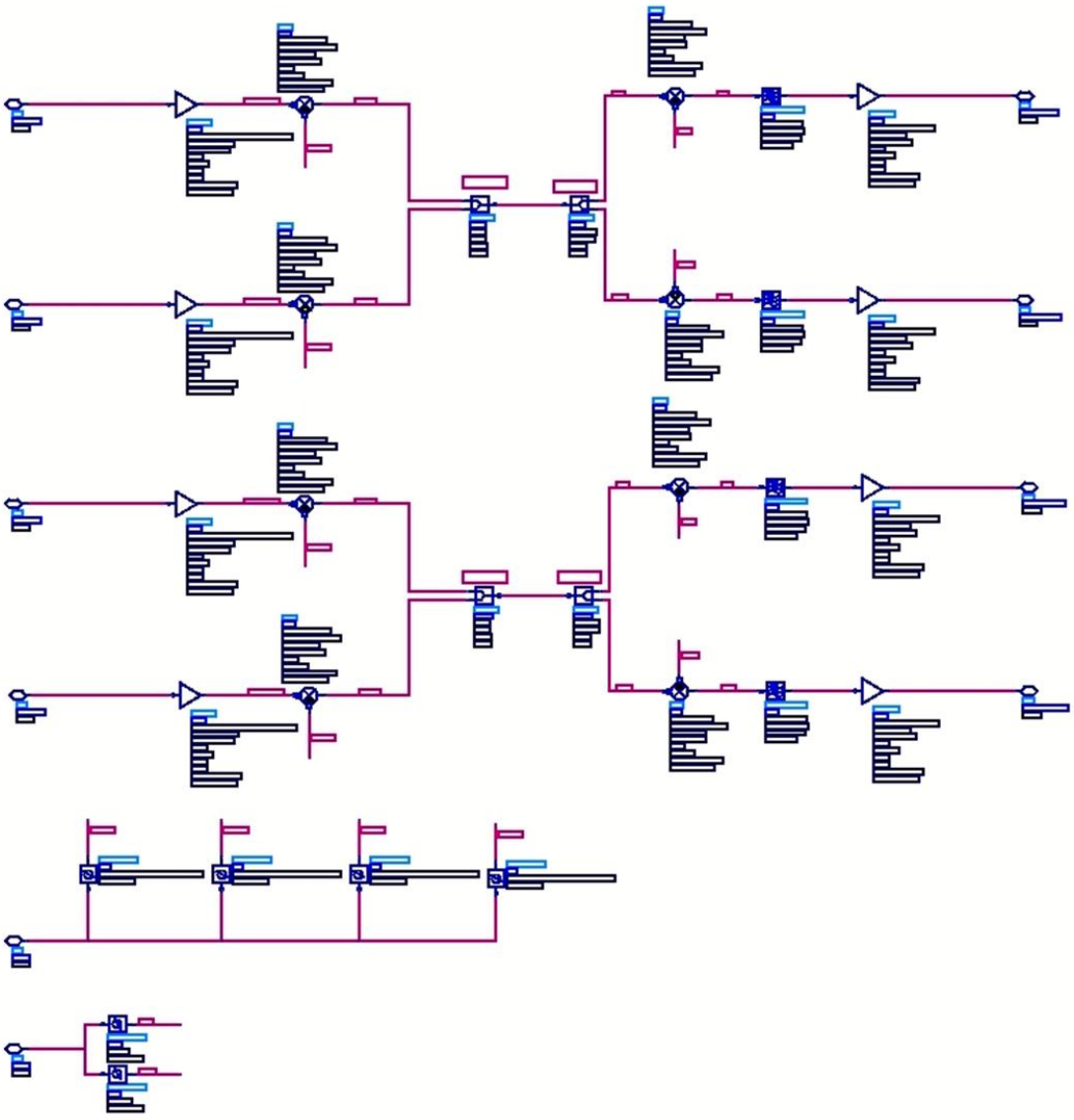

Fig. 3.14 System Behavioral Simulation in ADS

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Chapter 4

60-GHz Divide-by-4 Frequency Divider

4.1 Introduction

In mm-Wave phase-locked loops for LO generation, the first frequency divider is one of the most critical building blocks because of its highest operation frequency. As an attractive candidate, injection-locked frequency dividers (ILFDs) feature the highest operation frequencies and the lowest power. High-division-ratio ILFDs are desirable because they help reduce the number of divider stages, which would not only save power but also alleviate or even eliminate the problem with frequency alignment due to process variations and modeling inaccuracy. However, they typically exhibit much narrower locking range compared with that of divide-by-2 ILFDs due to the degradation of harmonic injection efficiency [1].

Recently, various techniques have been proposed to improve the locking range of divide-by-4 ILFDs. Varactor tuning with fine steps is used in LC-type ILFD [2], but it requires complicated calibration circuits. Inductive peaking [3] can improve injection efficiency, but the locking range improvement is still quite limited. RC-type ILFDs can achieve wide locking range and small area [4], but they are power hungry, and the output waveforms are quite distorted.

In this work, a simple but useful harmonic-boosting technique is proposed to enhance the locking range of divide-by-4 ILFDs. Section 4.2 introduces conventional

divide-by-4 ILFDs focusing on their limited locking range. Section 4.3 presents the proposed locking range enhancement technique by boosting the 3rd-order harmonic. The circuit implementation and measurements are discussed in Sections 4.4 and 4.5, respectively.

4.2 Conventional Divide-by-4 ILFDs

Fig. 4.1 shows a conventional divide-by-4 IFLD. The loading is based on LC tank with resonant frequency at ω_0. The self-oscillation is sustained by the cross-coupled pairs M_1 and M_2. Input signal is injected to the LC tank by M_3, whose gate bias can be set independently through AC coupling.

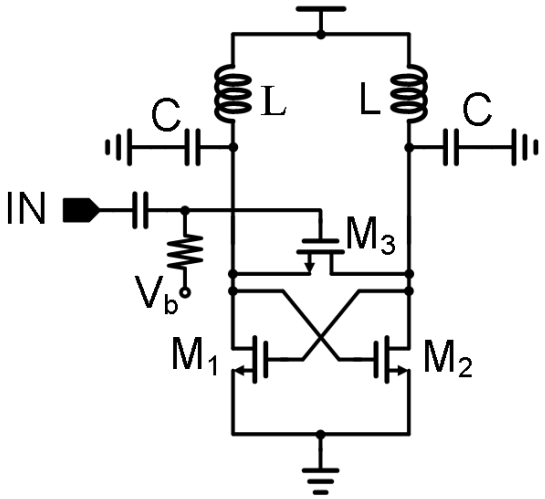


Fig. 4.1 Conventional divide-by-4 ILFD

The conventional divide-by-4 ILFD can be modeled as a feedback loop with a band-pass filter (BPF) composed of LC tank and a nonlinear single-balanced mixer, as shown in Fig. 4.2. At the output, the harmonics are filtered out by the BPF, and only the fundamental tone $v_{o,\omega}$ at a frequency close to the LC tank's self-oscillation frequency ω_0

is fed back to mix with both the input dc current I_{dc} and the input injection current i_{inj} at 4ω.

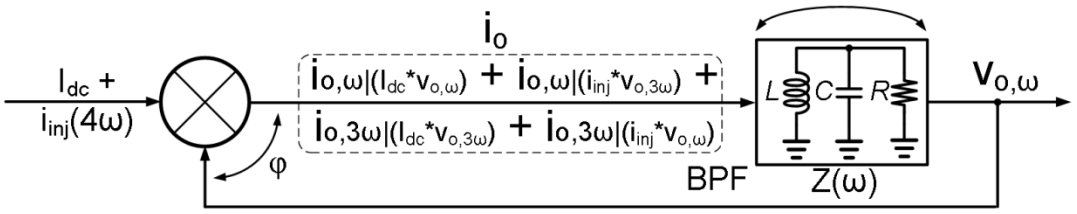


Fig. 4.2 Behavioral model of conventional divide-by-4 ILFD

Due to the hard switching and nonlinearities of the active devices, both fundamental mixing and harmonic mixing exist. $i_{o,\omega|(I_{dc}*v_{o,\omega})}$ and $i_{o,3\omega|(i_{inj}*v_{o,\omega})}$ are the mixing products of the fundamental tone with I_{dc} and i_{inj}, whose conversion coefficients are $k_{\omega|(I_{dc}*v_{o,\omega})}$ and $k_{3\omega|(i_{inj}*v_{o,\omega})}$, respectively. The corresponding equations are shown below:

$$i_{o,\omega|\left(I_{dc}*v_{o,\omega}\right)} = k_{\omega|\left(I_{dc}*v_{o,\omega}\right)} \cdot I_{dc} \cdot \cos\left(\omega t + \theta\right) \ , \tag{4.1}$$

$$i_{o,3\omega|\left(i_{inj}*v_{o,\omega}\right)} = k_{3\omega|\left(i_{inj}*v_{o,\omega}\right)} \cdot i_{inj} \cdot \cos\left(3\omega t - \theta\right) \ . \tag{4.2}$$

Simultaneously, $i_{o,\omega|(i_{inj}*v_{o,3\omega})}$ and $i_{o,3\omega|(I_{dc}*v_{o,3\omega})}$ are generated by mixing the 3rd-order harmonic of the output voltage with i_{inj} and I_{dc}, whose conversion coefficients are $k_{\omega|(i_{inj}*v_{o,3\omega})}$ and $k_{3\omega|(I_{dc}*v_{o,3\omega})}$, respectively. The corresponding equations are shown below:

$$i_{o,\omega|\left(i_{inj}*v_{o,3\omega}\right)} = k_{\omega|\left(i_{inj}*v_{o,3\omega}\right)} \cdot i_{inj} \cdot \cos\left(\omega t - 3\theta\right) \ , \tag{4.3}$$

$$i_{o,3\omega|\left(I_{dc}*v_{o,3\omega}\right)} = k_{3\omega|\left(I_{dc}*v_{o,3\omega}\right)} \cdot I_{dc} \cdot \cos\left(3\omega t + 3\theta\right) \ . \tag{4.4}$$

Proper operation of the ILFDs requires that the total phase shift around the loop is 0 and that the open-loop gain should be larger than unity, which is easily satisfied as long as the ILFD can self-oscillate.

As depicted by the phasor diagram in Fig. 4.3, the phase shift φ by the LC tank at ω should compensate the combined phase angle formed by the current components $i_{o,\omega|(I_{dc}*v_{o,\omega})}$ and $i_{o,\omega|(i_{inj}*v_{o,3\omega})}$. As ω moves further away from ω_0, |φ| becomes larger until it reaches the maximum value of $\arcsin(|i_{o,\omega|(i_{inj}*v_{o,3\omega})}|/|i_{o,\omega|(I_{dc}*v_{o,\omega})}|)$, which is proportional to $(k_{\omega|(i_{inj}*v_{o,3\omega})}/k_{\omega|(I_{dc}*v_{o,\omega})})\bullet\eta$, where η is the injection ratio defined as $|i_{inj}|/|I_{dc}|$. Normally, $|i_{o,\omega|(I_{dc}*v_{o,\omega})}|$ is designed to be the minimum value to sustain self-oscillation. So, without tuning ω_0, the locking range could be enhanced only by increasing $|i_{o,\omega|(i_{inj}*v_{o,3\omega})}|$, either by increasing $|i_{inj}|$ or $k_{\omega|(i_{inj}*v_{o,3\omega})}$. Larger $|i_{inj}|$ would require larger input power or larger injection device M_3, which are typically not desired. At the same time, $k_{\omega|(i_{inj}*v_{o,3\omega})}$ remains very small due to the 3rd-order harmonic mixing. As a result, $|i_{o,\omega|(i_{inj}*v_{o,3\omega})}|$ and thus the locking range are quite limited.

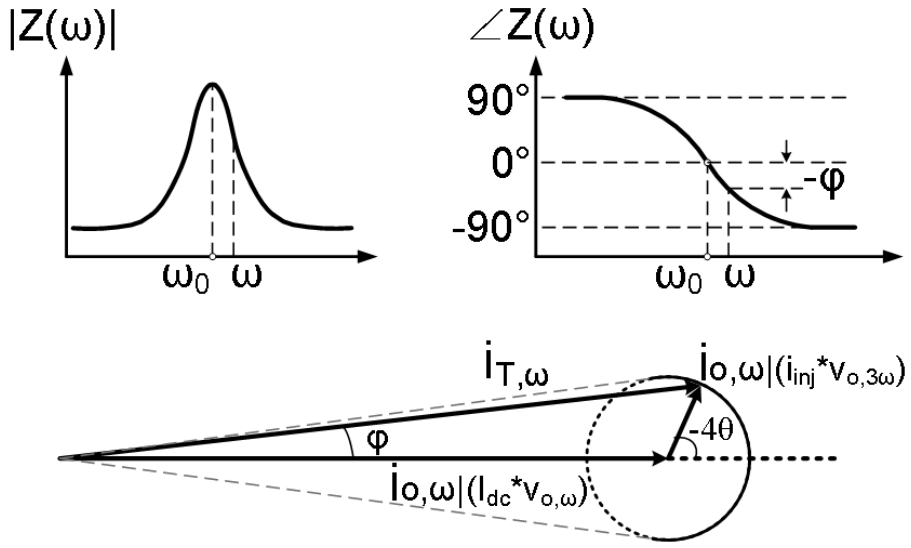


Fig. 4.3 Phasor diagram of conventional divide-by-4 ILFD

4.3 Proposed Locking Range Enhancement with Harmonic Boosting

In essence, the limited locking range of divide-by-4 ILFDs is attributed to weak harmonic mixing, whose efficiency is much lower than fundamental mixing. If the fundamental mixing could be employed to play the same role as the harmonic mixing to generate the desired tone, the locking range would be greatly enhanced. For divide-by-4 ILFDs, this could be done by adding another tone $v'_{o,3\omega}$ at frequency 3ω to the output, as shown by the behavioral model in Fig. 4.4.

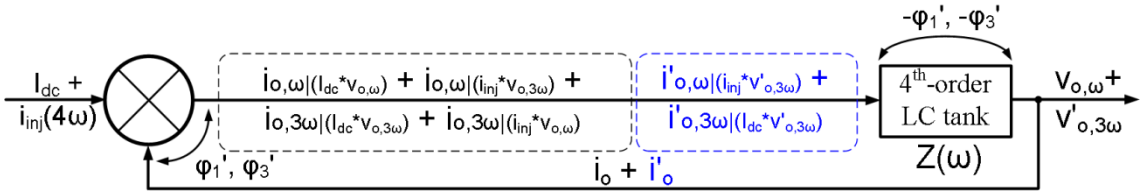


Fig. 4.4 Behavioral model of proposed locking range enhancement

By doing so, two additional terms $i'_{o,\omega|(i_{inj}*v'_{o,3\omega})}$ and $i'_{o,3\omega|(I_{dc}*v'_{o,3\omega})}$ are generated by fundamental mixing of $v'_{o,3\omega}$ with i_{inj} and I_{dc}, whose conversion coefficients $k'_{\omega|(i_{inj}*v'_{o,3\omega})}$ and $k'_{3\omega|(I_{dc}*v'_{o,3\omega})}$ are much larger than $k_{\omega|(i_{inj}*v_{o,3\omega})}$ and $k_{3\omega|(I_{dc}*v_{o,3\omega})}$, respectively. The corresponding equations are shown below:

$$i'_{o,\omega|(i_{inj}*v'_{o,3\omega})} = k'_{\omega|(i_{inj}*v'_{o,3\omega})} \cdot i_{inj} \cdot \cos(\omega t - \theta') \quad , \tag{4.5}$$

$$i'_{o,3\omega|(I_{dc}*v'_{o,3\omega})} = k'_{3\omega|(I_{dc}*v'_{o,3\omega})} \cdot I_{dc} \cdot \cos(3\omega t + \theta') \quad . \tag{4.6}$$

The phase condition at ω is analyzed with the phasor diagram in Fig. 4.5 (a), which indicates the maximum compensable phase shift $|\varphi_1'|$ would be significantly improved.

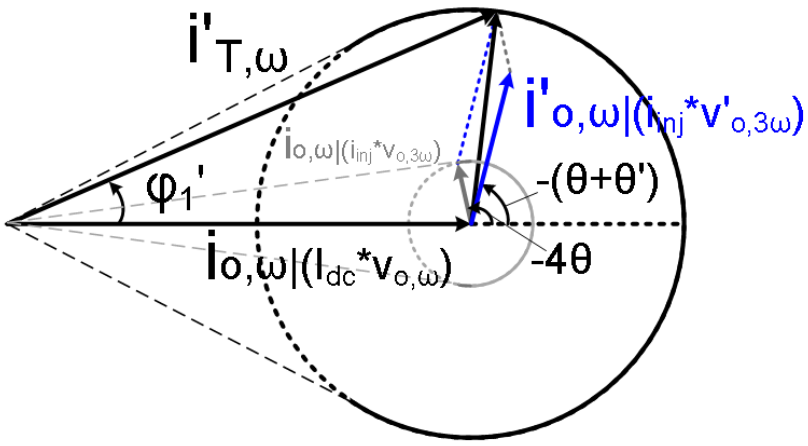


Fig. 4.5 Phasor diagram of proposed locking range enhancement at ω

As long as the 3rd-harmonic tone is boosted and becomes significant, the operation of the loop at 3ω needs to be analyzed. Theoretically, the total phase shift at 3ω in the loop should be 0, which is depicted by the phasor diagram in Fig. 4.6. Considering that $v'_{o,3\omega} < v_{o,\omega}$ and that the fundamental mixing has much higher efficiency than the harmonic mixing, it's typically true that:

$$i_{o,3\omega\,|(i_{inj}*v_{o,\omega})} > i'_{o,\omega\,|(i_{inj}*v'_{o,3\omega})} \gg i_{o,\omega\,|(i_{inj}*v_{o,3\omega})} \quad , \tag{4.7}$$

and

$$i_{o,\omega\,|(I_{dc}*v_{o,\omega})} > i'_{o,3\omega\,|(I_{dc}*v'_{o,3\omega})} \gg i_{o,3\omega\,|(I_{dc}*v_{o,3\omega})} \quad . \tag{4.8}$$

Therefore, the achievable range of $|\varphi_3'|$ is much wider than that of $|\varphi_1'|$ and thus the phase condition at 3ω is not a problem.

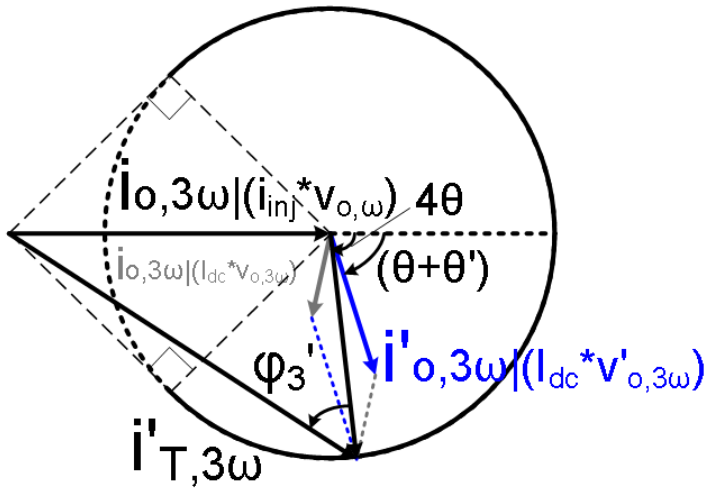


Fig. 4.6 Phasor diagram of proposed locking range enhancement at 3ω

The coexistence of two tones can be implemented by simply using a 4th-order LC tank shown in Fig. 4.7 with two intrinsic impedance peaks at ω_0 and $3\omega_0$. To enhance locking range, $|Z(3\omega_0)|$ is desired to be large. But at the same time, $|Z(3\omega_0)|$ should be sufficiently smaller than $|Z(\omega_0)|$ to ensure stable fundamental oscillation. Taking these two factors into account, $|Z(3\omega_0)|$ is designed to be 3/4 of $|Z(\omega_0)|$. Besides, depending on different applications, $|Z(3\omega_0)|$ may need to be further scaled down so that the boosted 3rd-order tone $v'_{o,3\omega}$ would not affect the operation of the next stages. Fortunately, the following stages are typically dividers with input locking range around $\omega/4$ and thus would not be affected by $v'_{o,3\omega}$. LC-based buffers with intrinsic band-pass characteristic can also be inserted to filter out this harmonic if necessary.

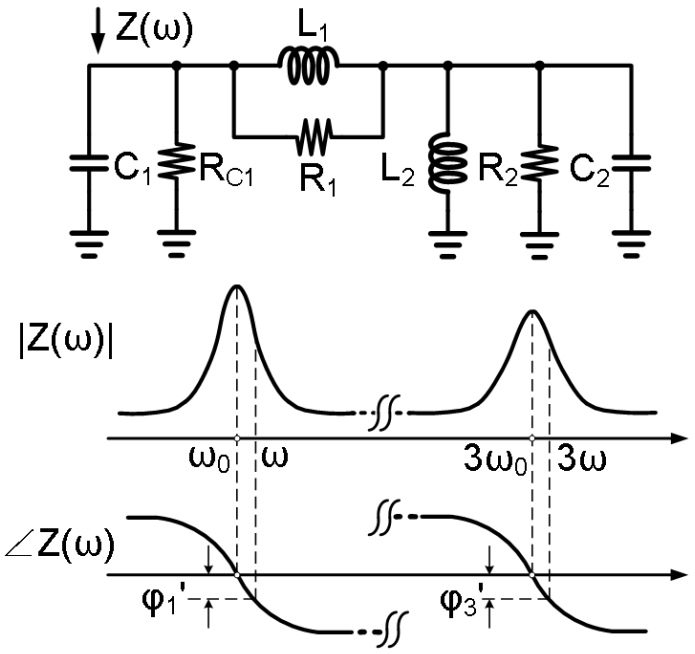


Fig. 4.7 Proposed 4th-order LC tank and its impedance plots

4.4 Circuit Design and Implementation

Fig. 4.8 shows the schematic of 60-GHz divide-by-4 ILFD with the proposed locking range enhancement technique. Self-oscillation is sustained by cross-coupled pair M_1 and M_2. With ac coupling, M_3 is biased in the sub-threshold region to further boost up the 3rd-order harmonic for injection to the LC tank.

The 4th-order tank, composed of $L_{1\pm}$, $L_{2\pm}$, $C_{1\pm}$ and $C_{2\pm}$, has two impedance peaks at around 16GHz and 48GHz. As shown in Fig. 4.9, L_{1+} and L_{1-} are separated to minimize their capacitive coupling and thus contribute minimum capacitance to $C_{1\pm}$ while L_{2+} and L_{2-} are combined to form a differential coil to save area. All of these inductors are implemented with top thick metal layer to improve quality factor. Simulated in ADS Momentum, $L_{1\pm}$ has inductance of 300pH while $L_{2\pm}$ has inductance of 500pH.

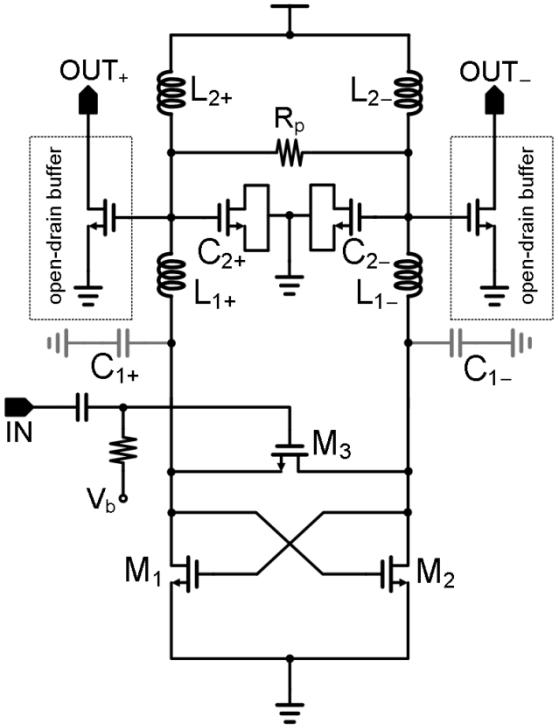


Fig. 4.8 Schematic of the proposed divide-by-4 ILFD

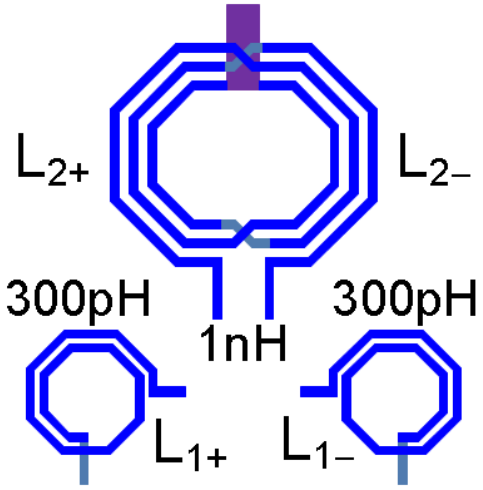


Fig. 4.9 Layout of the inductors

$C_{1\pm}$ is purely contributed by the parasitic capacitance, and $C_{2\pm}$ is implemented with gate capacitance of NMOS FETs. The resistor R_p is used to lower the impedance $|Z(\omega_0)|$

without affecting $|Z(3\omega_0)|$ much. Again, $|Z(3\omega_0)|$ is designed to be around 3/4 of $|Z(\omega_0)|$. Open-drain buffers are included for testing purposes.

4.5 Experimental Results

The proposed ILFD has been designed and fabricated in a 1P6M LP 65-nm CMOS process. The micrograph of the whole chip is shown in Fig. 4.10, and the core area is 0.16×0.26 mm^2.

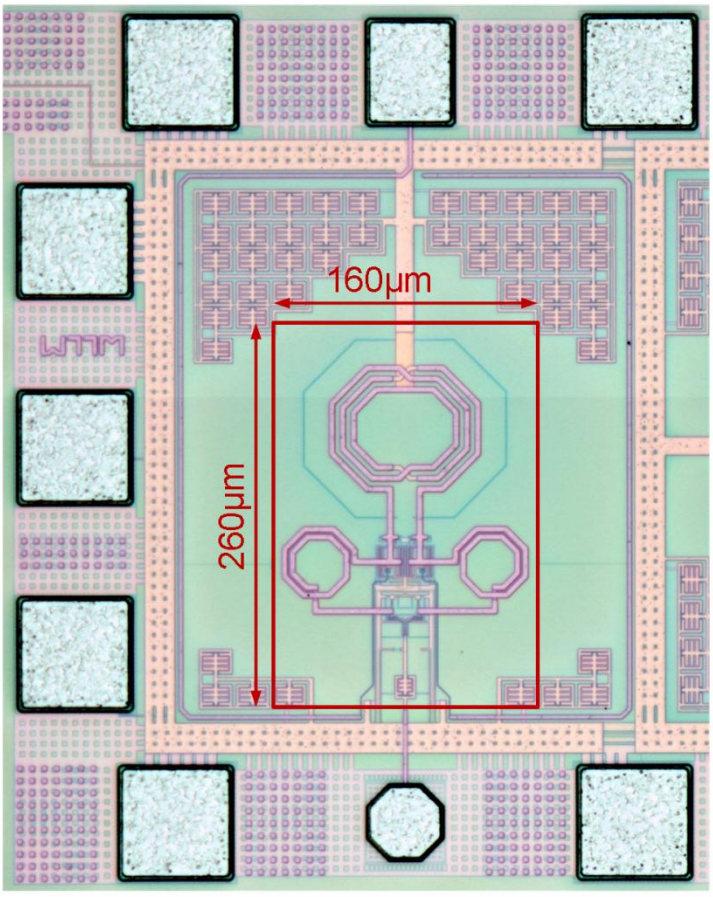


Fig. 4.10 Chip micrograph of the proposed divide-by-4 ILFD

4.5.1 Measured Sensitivity Curves

Fig. 4.11 reports the measured sensitivity curves. With 0dBm input signal, the proposed ILFD measures a locking range of 21.9% from 58.53GHz to 72.92GHz while consuming 3.6mA current from a 0.6-V supply.

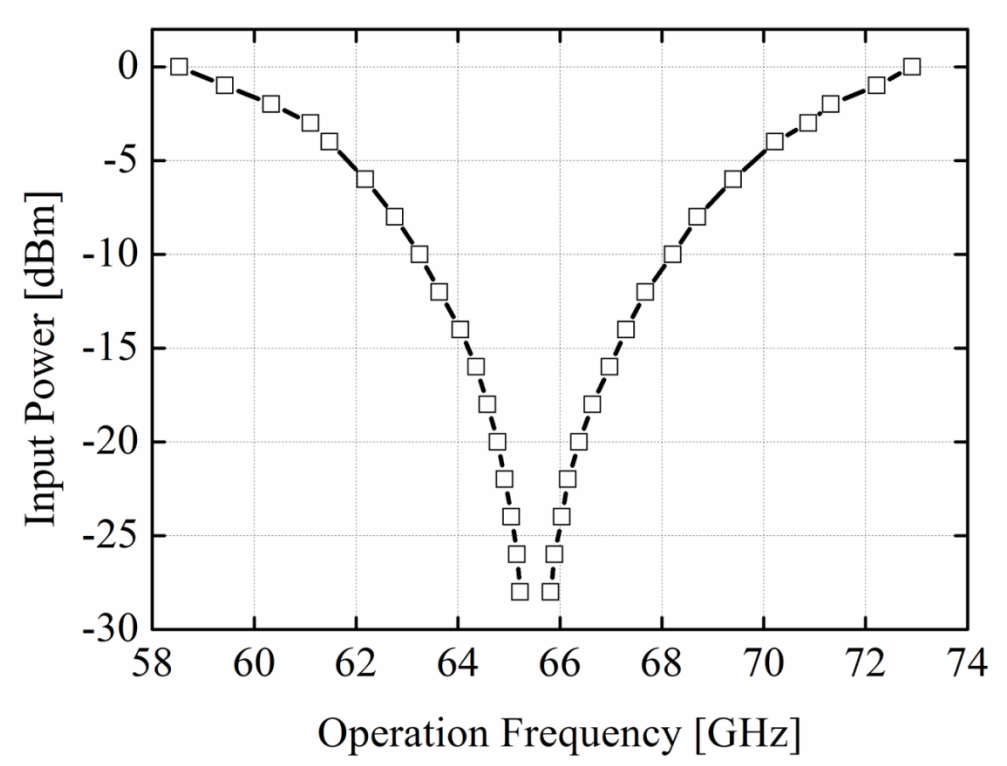


Fig. 4.11 Measured sensitivity curves

4.5.2 Measured Phase Noise

To measure the phase noise, the input 60-GHz signal is first down-converted by an external V-band harmonic mixer and measured with a spectrum analyzer while the output 15-GHz signal is directly measured. As shown in Fig. 4.12, the phase noise at the divider's output is around 12 dB lower than that of the input signal, as expected theoretically.

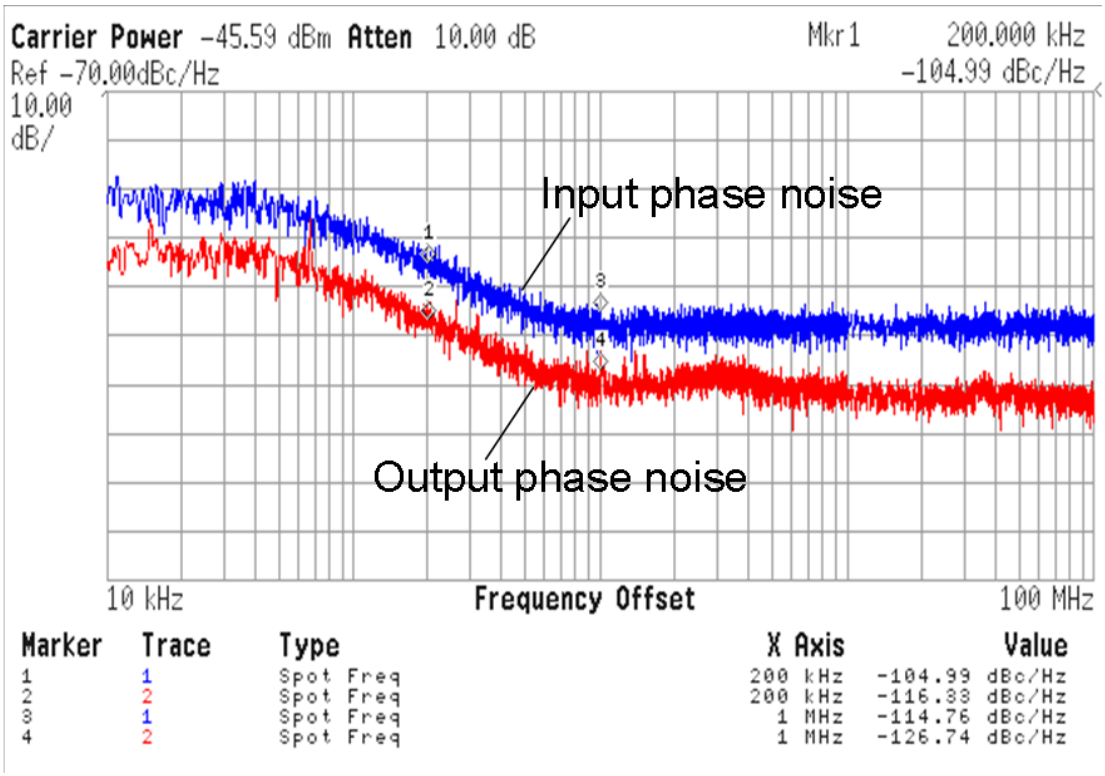


Fig. 4.12 Measured phase noise at the proposed ILFD's input and output

4.5.3 Measured Output Spectrum

The output spectrum has two tones, as shown in Fig. 4.13. The power of the 3rd-order harmonic at 45GHz is around 5.5 dBm lower than that of the fundamental tone at 15GHz. From another perspective, the 3rd-order harmonic tracks the input signal so well that the proposed divider can also achieve division ratio of 4/3. These two tones have such a large frequency difference that the unwanted tone would get significantly attenuated by the band-pass filtering nature of the following stages.

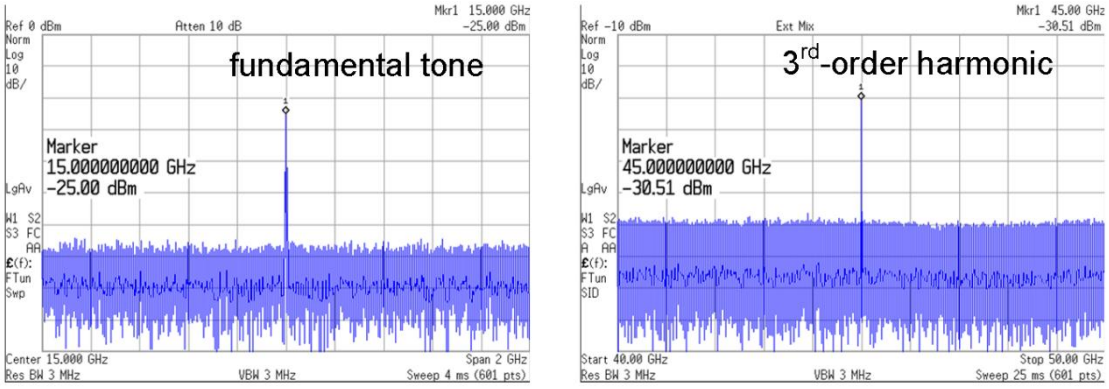


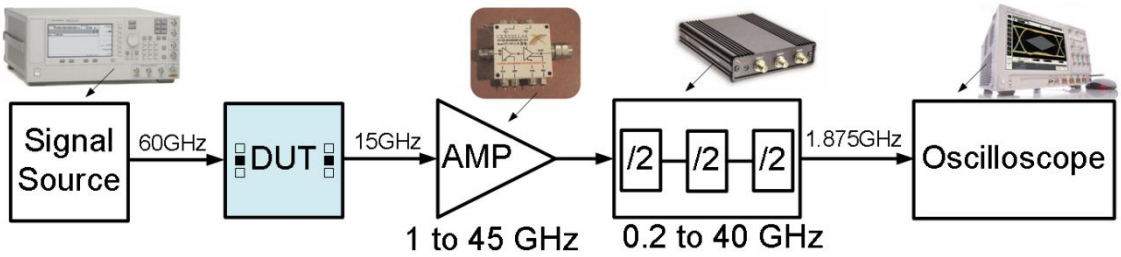
Fig. 4.13 Measured output spectrum

4.5.4 Measured Output Transient Waveform

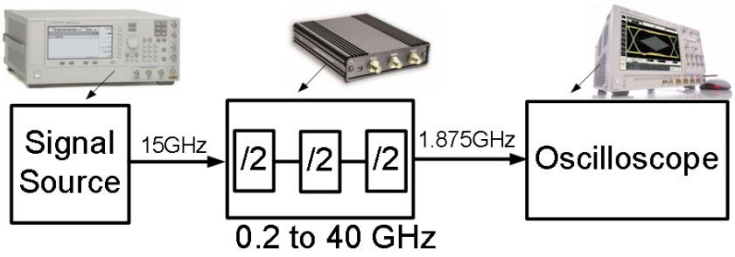
In general, the first divider in a phase-locked loop (PLL) drives a frequency divider chain to produce a low frequency replica of the VCO output. To verify that the harmonic boosting technique would not affect the function of the following divider chain, a setup has been built, as shown in Fig. 4.14 (a). The input of the proposed divider (DUT) is driven with a signal source at 60GHz. Due to the loss of the open-drain buffers and the connection cables, the output power of DUT is not large enough to directly drive an off-chip three cascaded stages of divide-by-2 dividers. Therefore, an off-chip amplifier with respective gain of 21dB and 17dB at 15GHz and 45GHz is inserted between the DUT and the divider chain. For comparison, another setup with sinusoidal source input at 15GHz also has been built, as shown in Fig. 4.14 (b).

The two output waveforms observed by the oscilloscope shown in Fig. 4.14 (c) are almost the same, which indicates the boosted 3rd-order harmonic of proposed divider doesn't affect the operation of the following divider chain. Fortunately, on-chip divider

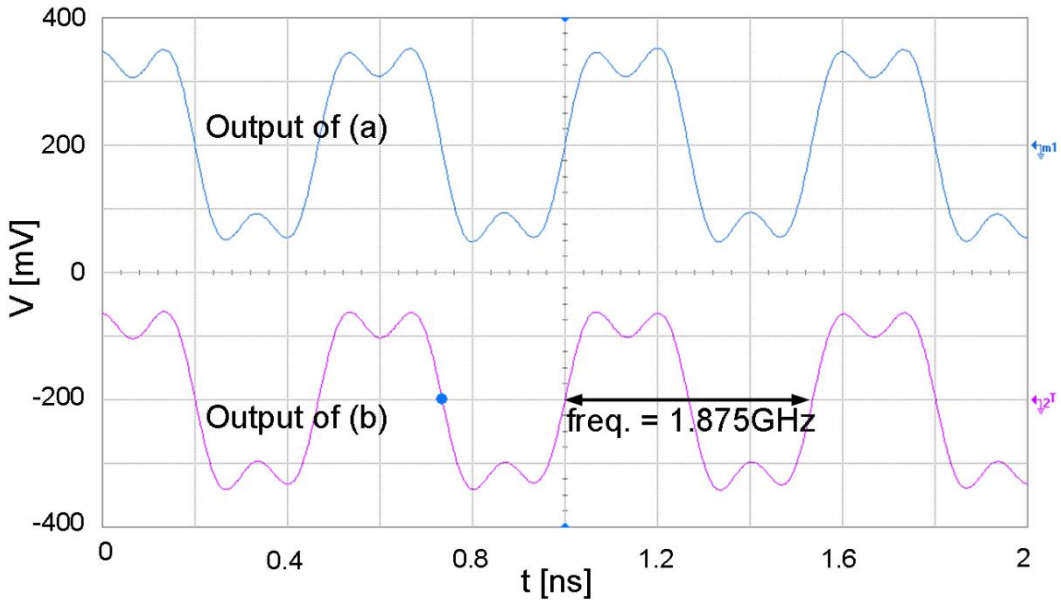
chain normally has a much smaller input frequency range than the off-chip one used here, and thus the situation is expected to be even better.



(a)



(b)



(c)

Fig. 4.14 Setups of a divider chain driven by (a) proposed divider and (b) sinusoidal source, and (c) their output transient waveforms.

4.5.5 Performance Summary

Table 4.1 summarizes the performance of the proposed divide-by-4 ILFD and compares against with that of recently reported state-of-the-art mm-Wave high-division-ratio dividers. Without any frequency tuning, the divide-by-4 ILFD in this work achieves the widest locking range while consuming the lowest power, resulting in the highest figure of merit (FoM) of 6.54. The FoM is defined as:

$$FoM = \frac{Locking\ Range\ |_{GHz}}{Power\ |_{mW}} \quad . \tag{4.8}$$

Table 4.1 Performance summary and comparison of mm-Wave high-division-ratio dividers

Ref.	Ratio	Type	f_{min} [GHz]	f_{max} [GHz]	Locking Range [GHz] / [%]	Supply [V]	Power [mW]	FoM	Technology
This Work	4	LC	58.5	72.9	14.4 / 21.9	0.6	2.2	6.54	65nm CMOS
[1]	4	LC	79.7	81.6	1.9 / 2.4	0.56	12.4	0.15	65nm CMOS
[2]	4	LC	70.0*	71.6*	1.6 / 2.3	0.5	2.75	0.58	90nm CMOS
[3]	4	LC	57.4	59.8	2.4 / 4.1	1.8	12.6	0.19	180nm CMOS
[4]	4	RC	63.5*	70.0*	6.5 / 9.7	1.0	6.5	1.00	65nm CMOS
[5]	3	LC	55.7*	57.8*	2.1 / 3.7	1.0	3.12	0.67	130nm CMOS
[6]	3	LC	58.6	67.2	8.6 / 13.7	1.0	5.2	1.65	65nm CMOS

* Sub-band with the highest frequency is chosen for comparison.

4.6 Conclusion

Harmonic boosting with 4th-order LC tank is proposed in this work to implement LC-type divide-by-4 ILFD with wide locking range at mm-Wave frequencies. Demonstrated in 65-nm CMOS process, a locking range of 21.9% from 58.53GHz to

72.92GHz is achieved, with power consumption of 2.2mW, resulting FoM of 6.54, which is much better than conventional high-division-ratio dividers.

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Chapter 5

60-GHz Transformer-Based Quadrature VCO

5.1 Introduction

With recent advancement in nanometer-scale CMOS technologies, mm-Wave CMOS LC VCOs have become realizable. However, their frequency tuning range is still quite limited because existing RF frequency tuning mechanisms are no longer suitable. At mm-Wave frequencies, conventional varactor tuning significantly degrades the spectral purity due to inferior quality factor of varactor and more severe AM-PM noise conversion. The situation is only exacerbated when the desired tuning range needs to be wide enough to cover PVT variations in addition to the allocated frequency bands. Transconductor tuning [1] can help extend the tuning range, but the performance in terms of phase noise and power consumption is significantly degraded.

A bimodal enhanced-magnetic-tuning technique is proposed in this work to tune the oscillation frequency of mm-Wave QVCOs. Section 5.2 describes and compares the existing magnetic tuning technique and the proposed enhanced magnetic tuning technique. Section 5.3 discusses the bimodal operation by tuning the polarity of the phase shift. In Section 5.4, the proposed bimodal enhanced-magnetic-tuning technique is demonstrated in a V-band QVCO. Section 5.5 presents the experimental results, , and conclusions are drawn in Section 5.6.

5.2 Proposed Enhanced-Magnetic-Tuning Technique

Existing magnetic tuning was proposed in [2] to tune VCOs at RF frequencies, as shown in Fig. 5.1.

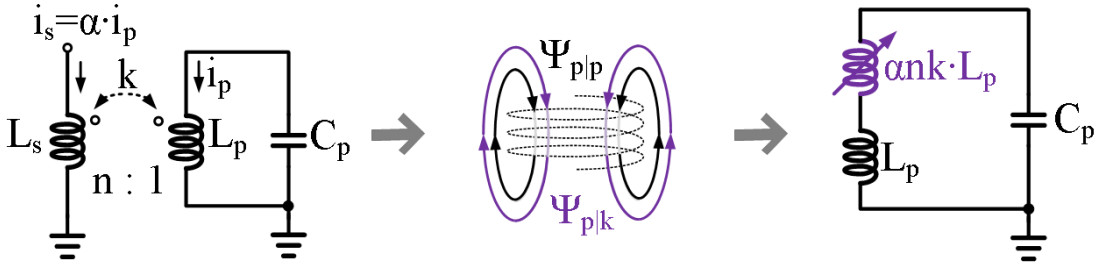


Fig. 5.1 Conventional magnetic tuning

The total magnetic field in the primary coil is comprised of two components: a self-induced magnetic field $\Psi_{p|p}$ due to the current i_p flowing through the primary coil L_p, and another magnetic field $\Psi_{p|k}$ induced through magnetic coupling by the current i_s flowing through the secondary coil L_s. By fixing i_p and varying i_s, $\Psi_{p|p}$ is kept constant while $\Psi_{p|k}$ is variable. Intuitively, the variable magnetic field $\Psi_{p|k}$ determines the frequency tuning range. Quantitatively, assuming that i_s and i_p are either in-phase or out-of-phase so that $\alpha = i_s/i_p$ is real, $\Psi_{p|k}$ can be modeled as variable inductor with inductance of α n k L_p, which clearly shows that the frequency can be tuned by varying α, depending on the magnetic coupling factor k and the turn ratio n. At RF frequencies, k can be as high as 0.85 for an on-chip spiral transformer with turn ratio of 1.4 [2]. However, the maximum achievable k is much smaller at mm-Wave frequencies, resulting in smaller variable range of $\Psi_{p|k}$ and thus narrower frequency tuning range. One potential way to compensate the degradation of k is to increase n by using a larger L_s. Unfortunately, this would increase the parasitic capacitance, which draws more current and reduces the effective i_s. Worse yet, k is typically decreased as n is increased

due to layout limitation. As a result, VCOs with magnetic tuning still have limited frequency tuning range at mm-Wave frequencies.

To overcome the limitations of the existing magnetic tuning technique, a more effective "enhanced magnetic tuning" technique is proposed in this work, as shown in Fig. 5.2, in which the second coil is also connected directly to the primary coil. As such, the tunable current i_s is also redirected through L_p to generate an additional variable magnetic field $\Psi_{p|s}$ and superimpose on $\Psi_{p|k}$ to increase the total tunable magnetic field such that the effective variable inductance becomes α (1 + n k) L_p, which is α L_p larger than that with the conventional magnetic tuning. This improvement is significant because n k is typically less than 1 at mm-Wave frequencies as discussed above.

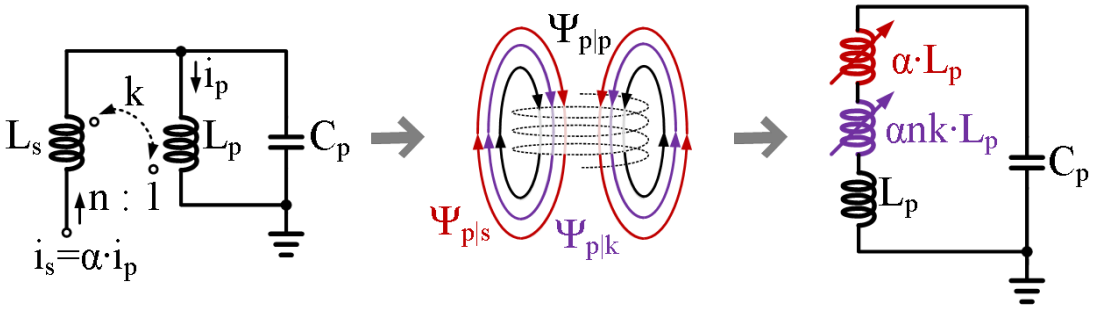


Fig. 5.2 Proposed Enhanced magnetic tuning

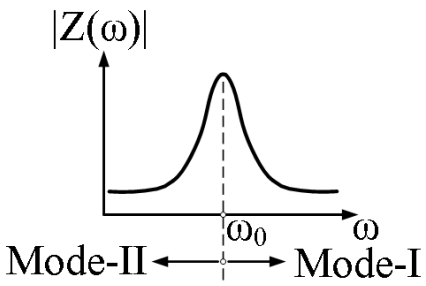
The resonant frequency of proposed enhanced magnetic tuning can be easily derived as:

$$\omega = 1/\sqrt{\left[1+\alpha\left(1+n\cdot k\right)\right]L_pC_p} \quad . \tag{5.1}$$

where C_p is the capacitance of the resonant tank.

5.3 Proposed Bimodal Operations

The assumption that α is a real number can be realized by connecting two identical differential VCOs as a QVCO. Intrinsically it has two possible IQ phase sequences with the I signal either leading or lagging the Q signal by 90 °corresponding to $\alpha < 0$ and $\alpha > 0$, respectively. As shown in Fig. 5.3, the resonant frequency locates either in a higher band or in a lower band around the center frequency ω_0 of the LC tank, depending on the polarity of α. In the following analysis, these two operation modes are defined as Mode-I and Mode-II, respectively.



Modes	$\angle I - \angle Q$	$\alpha = i_s/i_p$	ω
Mode-I	$+90°$	< 0	$\omega > \omega_0$
Mode-II	$-90°$	> 0	$\omega < \omega_0$

Fig. 5.3 Two operation modes of QVCO

Conventionally, since the LC tank is asymmetrical and since the capacitive and resistive parasitics of the circuits introduce some delay to the coupling paths between the two coupled oscillators [3], the phase sequence of a QVCO is typically limited to Mode-I only, and the oscillation frequency is typically higher than the center frequency of LC tank.

Intuitively, if both Mode-I and Mode-II operations can be employed, the oscillation frequency range would be expected to be doubled. Mode-I operation can be selected by the phase delays in the coupling paths of QVCO to make I lead Q. On the other hand, Mode-II operation can be implemented by introducing phase advances in the coupling paths to make I lag Q. In other words, by controlling the polarity of the phase shift to properly select the IQ sequence, bimodal operation can be achieved.

As shown by the model in Fig. 5.4, –φ represents the negative phase shift introduced by the parasitic resistance and capacitance, while the 90° phase shift is inserted intentionally by controlling the switch SW.

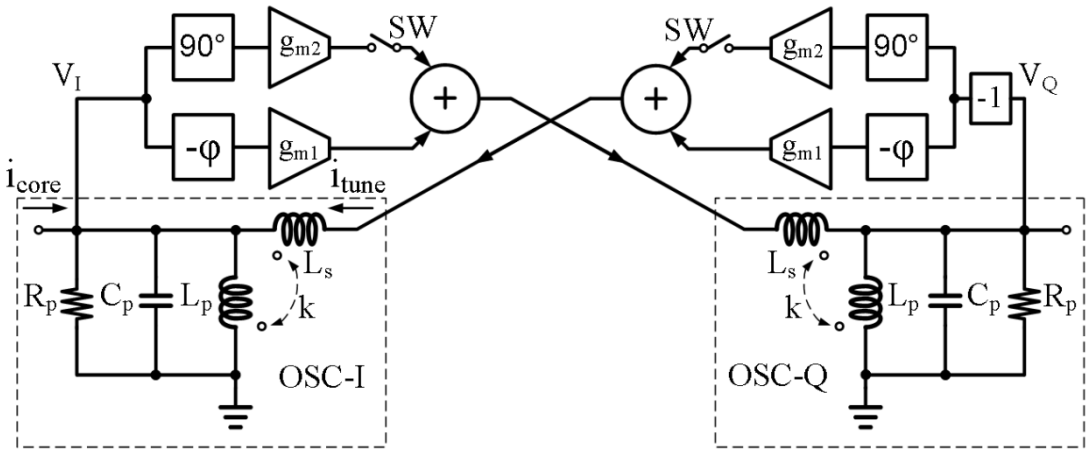


Fig. 5.4 Behavioral mode of proposed QVCO with mode selection

With SW turned off, the phase shift –φ is negative, and the total current of Mode-I is larger than that of Mode-II, i.e. $i_{t,Mode\text{-}I} > i_{t,Mode\text{-}II}$. Consequently, Mode-I is selected because it requires less energy, as illustrated by the phasor diagram in Fig. 5.5 (a). On the contrary, with SW on, the inserted 90° phase shift compensates the parasitic phase shift –φ, and thus the total phase shift becomes positive. As such, the total current of Mode-II is larger than that of Mode-I, i.e. $i_{t,Mode\text{-}II} > i_{t,Mode\text{-}I}$, as illustrated in Fig. 5.5 (b),

and Mode-II operation is achieved. In each mode of operation, the enhanced magnetic tuning is applied, in which the frequency tuning is done by continuously tuning the current i_{tune} while the oscillation is sustained by the current i_{core}.

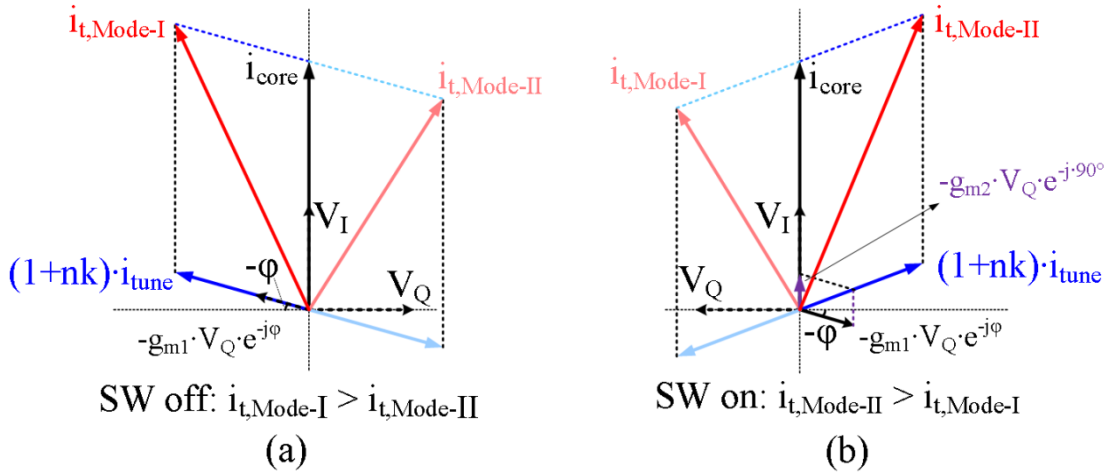


Fig. 5.5 Phasor diagram of Mode I and mode II operations

5.4 Circuit Design and Implementation

Fig. 5.6 shows the schematic of QVCO with proposed bimodal enhanced magnetic tuning. Cross-coupled transistors $M_{1,2}$ implement the negative transconductance. $M_{3,4}$ and $M_{5,6}$ realize the coupling transconductance without and with 90° phase shift, respectively. $M_{5,6}$ are sized about 1/2 of $M_{3,4}$ to save power while still having enough strength to guarantee that the total phase shifts are positive when the tail current I_{mode} is on to enable $M_{5,6}$. The 90° phase shift is simply obtained with an LC-based amplifier stage, whose center frequency is much lower than the QVCO oscillation frequency.

For each differential oscillator, L_p and L_s are implemented by a differential coil with a center tap to save area and to maximize quality factor. L_p has one turn while L_s has two turns, and they are interleaved to maximize the magnetic coupling factor, as

shown in Fig. 5.7. Simulated in ADS Momentum at 60GHz, Lp and Ls are 50nH and 120nH with quality factor of 15 and 22, respectively, and their coupling factor is around 0.4.

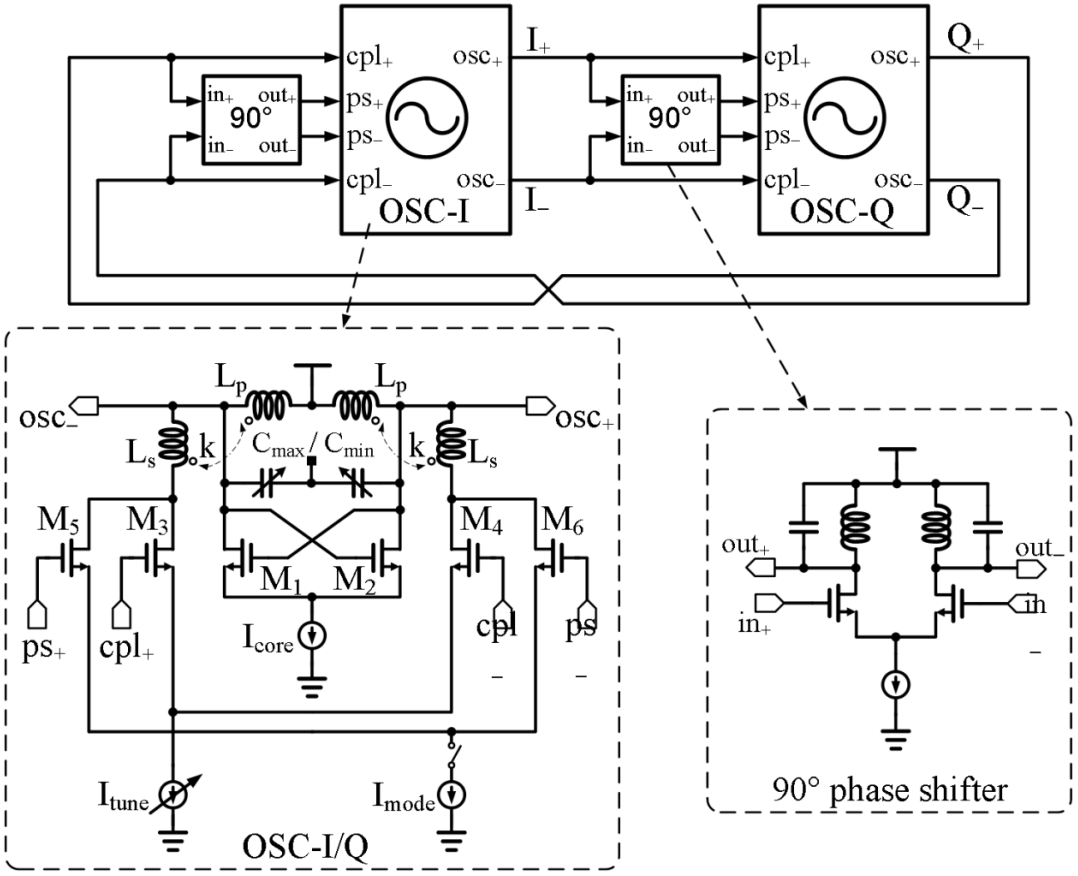


Fig. 5.6 Schematic of QVCO with bimodal enhanced magnetic tuning

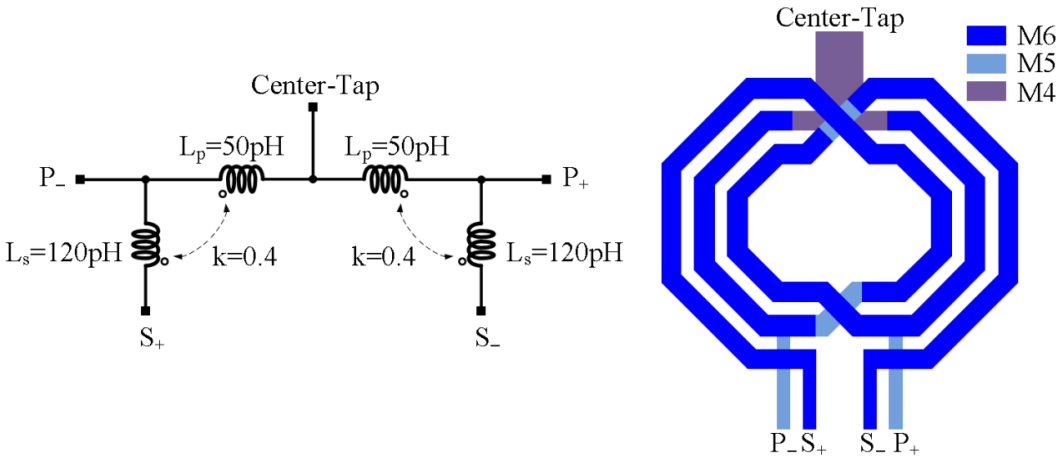


Fig. 5.7 Layout of transformer

5.5 Experimental Results

The proposed QVCO with bimodal enhanced magnetic tuning has been designed and fabricated in a 1P6M LP 65nm CMOS technology. Fig. 5.8 shows the photograph of the prototype which occupies a core area of 0.45×0.25 mm^2.

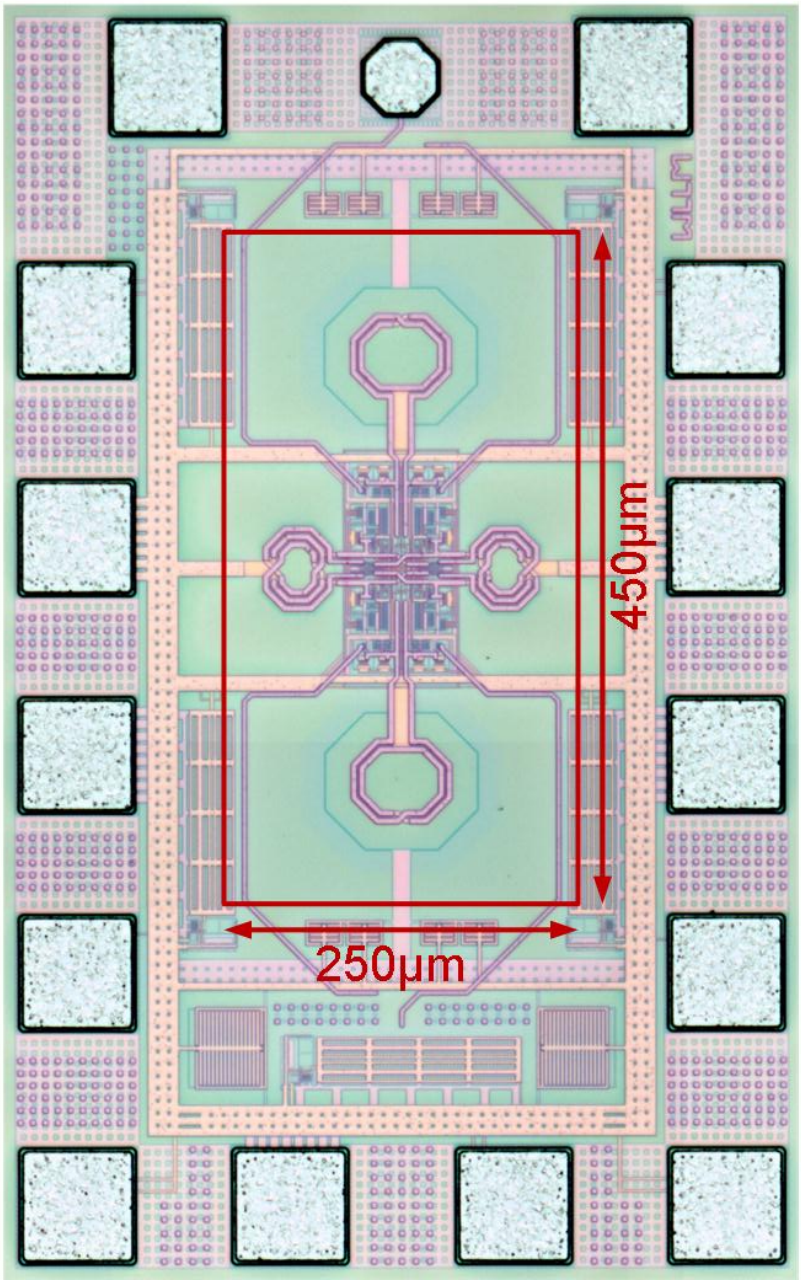


Fig. 5.8 Chip micrograph of the proposed QVCO

5.5.1 Measured Frequency Tuning Curves

The measured frequency tuning curves are shown in Fig. 5.9. There are 4 over-lapping sub-bands thanks to the bimodal operation and 1-bit digitally controlled varactor. The frequency can be tuned continuously from 48.8GHz to 62.3GHz. With 1.2-V supply, the current consumption varies from 13mA to 25mA as the tuning current varies.

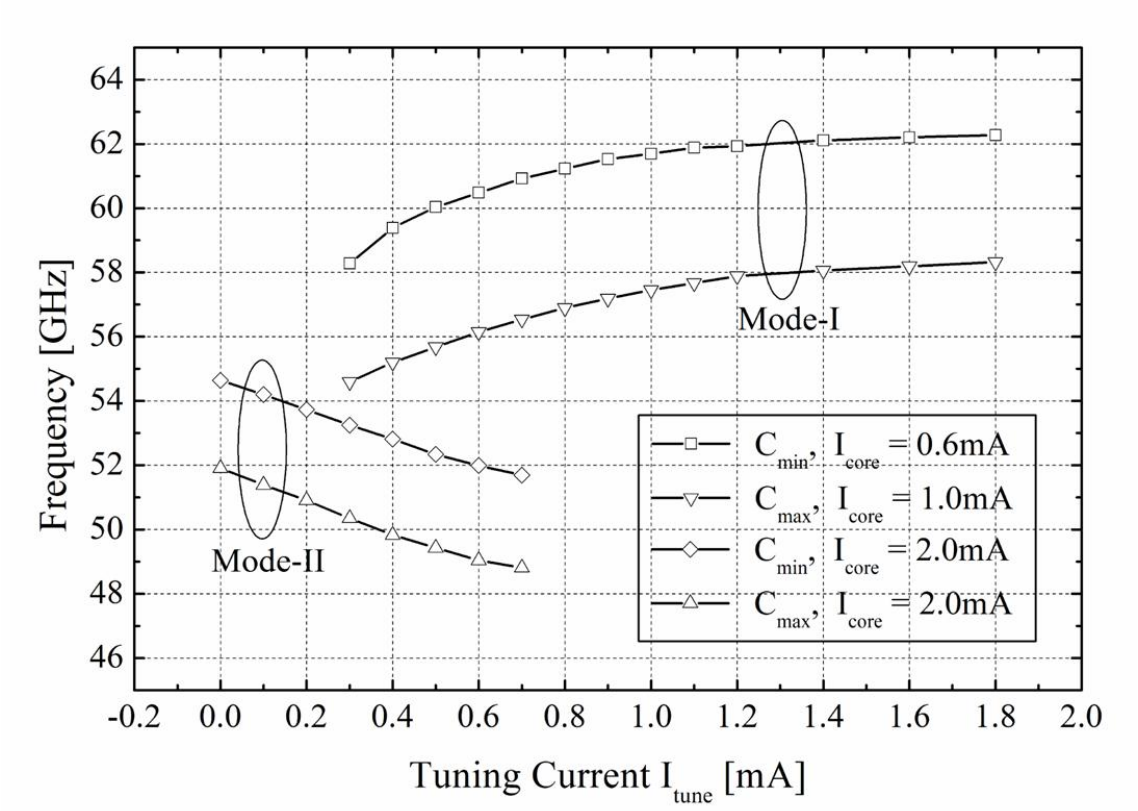


Fig. 5.9 Measured frequency tuning curves

5.5.2 Measured Phase Noise

To measure the phase noise, the output signals of the QVCO are down-converted by external Q-band and V-band harmonic mixers. Assuming the phase noise contributed

by the mixers is negligibly small, the phase noise values at 48.8GHz, 55.6GHz, and 62.3GHz are measured to be –94, –90 and –92 dBc/Hz at 1MHz offset, as reported in Fig. 5.10. The difference of the noise floor is due to the different input power level to the spectrum analyzer, considering different conversion loss of the mixers and different output power of the QVCO at different frequencies.

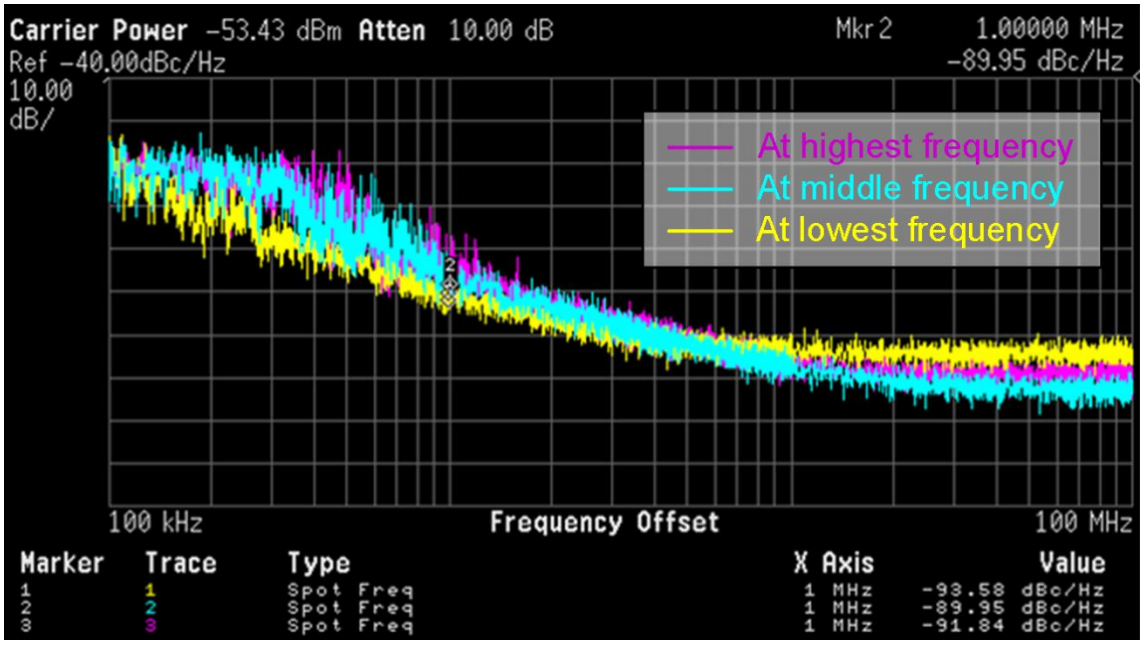


Fig. 5.10 Measured phase noise performance

5.5.3 Measured Output Spectrum

When the proposed QVCO oscillates at the highest frequency, the output spectrum is shown in Fig. 5.11.

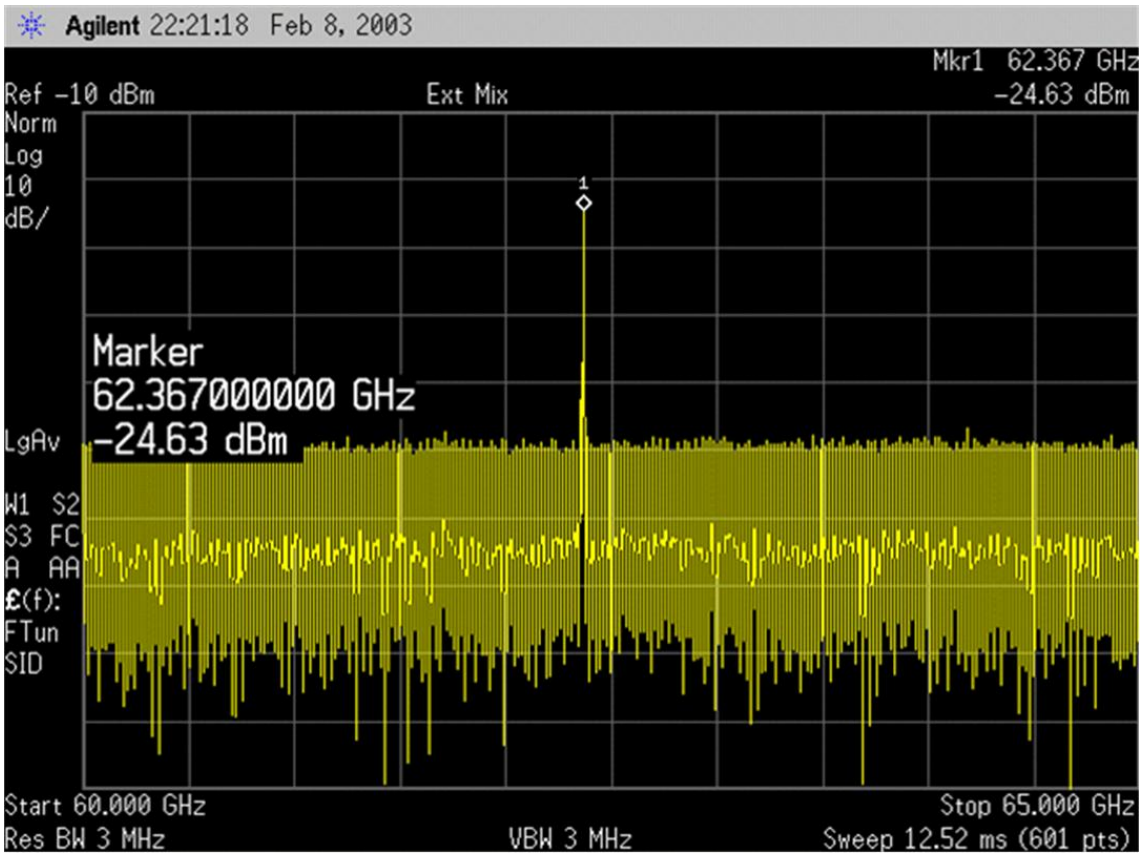


Fig. 5. 11 Measured output spectrum

5.5.4 Performance Summary

Table 5.1 summarizes the performance of the proposed QVCO and compares with that of some recently published state-of-the-art mm-Wave QVCOs. With proposed bimodal enhanced magnetic tuning, the QVCO achieves a wide tuning range of 24%, FoM from 173dBc to 176dBc, and FoM_T from 181dBc to 184dBc.

$$FoM = 10\log_{10}\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\cdot P_{diss}\,|_{mW}}\right] \tag{5.2}$$

$$FoM_T = FoM + 20\log_{10}\left(\frac{TR\,|_{\%}}{10}\right) \tag{5.3}$$

Table 5.1 Performance summary and comparison of mm-Wave QVCOs

Ref.	This work	JSSC 2008 [4]	ISSCC 2009 [5]	ISSCC 2011 [6]	JSSC 2011 [7]
f_{min} [GHz]	48.8	43.7	57.1	56.0	54.0
f_{max} [GHz]	62.3	51.7	66.1	60.35	61.0
TR [GHz]/[%]	13.5 / 24.3	8.0 / 16.8	9.0 / 14.6	4.35 / 7.4	7.0 / 12.2
P.N. @1MHz [dBc/Hz]	-90.0 ~ -94.0	-85.0	-75.0	-95.0 ~ -97.0	-85.0
Supply [V]	1.2	1.0	1.1	1.0	1.0
Power [mW]	15.6 ~ 30.0	19.0 ~ 32.0	26.5	22.0	14.9
FoM [dBc]	173 ~ 176	164 ~ 166	157	177 ~ 179	170
FoM_T [dBc]	181 ~ 184	168 ~ 170	160	174 ~ 176	172
Tuning Mechanism	Bimodal Enhanced Magnetic Tuning	Coupling Current Tuning	Varactor Tuning	Varactor Tuning	Varactor Tuning
Technology	65nm CMOS	90nm CMOS	45nm CMOS	65nm CMOS	65nm CMOS

5.5.5 Other Simulated Performance

5.5.5.1 Output Voltage Swing

According to the simulation, the output voltage swing (peak-to-peak) varies from 350mV to 600mV. By properly sizing the input device of the injection-locked frequency divider, the QVCO is able to directly drive the divider. Because even though the frequency dividers are measured individually with 0-dBm input power (630mV peak-to-peak for 50Ω), the loss due to unmatched impedance, pads and routing wires would make the actual power available to the divider smaller than 0 dBm. For some dividers

which require much larger input voltage swing, a buffer can be inserted between QVCO and divider.

5.5.5.2 I/Q Mismatches

For QVCO at RF frequencies, the I/Q mismatches can be measured with on-chip single side band mixer (SSB). At 60-GHz, the device size of the SSB should be small to avoid degradation of frequency tuning range. Therefore, the phase error contributed by SSB is not negligible because the matching of small devices is typically bad. Besides, the asymmetry of signal routings also contributes significant phase error. Therefore, SSB is not able to accurately measure the I/Q mismatches of 60-GHz QVCO.

Post-simulation shows that the I/Q mismatches are within the range from 0.3° to 4.5°.

5.6 Conclusion

A novel bimodal enhanced-magnetic-tuning technique is proposed in this work to implement QVCO with wide tuning range at mm-Wave frequencies. Demonstrated in 65nm CMOS process, a wide tuning range of 24% from 48.8GHz to 62.3GHz is achieved, with phase noise lower than -90dBc at 1MHz offset, resulting FoMT from 181 to 184 dBc, which is much better than conventional QVCOs with much smaller frequency tuning ranges.

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Chapter 6

24-GHz and 60-GHz Dual-Band Standing-Wave VCO

6.1 Introduction

With recent advances in CMOS technology, mm-Wave circuits become more and more attractive for many interesting applications such as vehicle radars at 77 GHz and 24 GHz and communication systems at 60 GHz and 24 GHz. Moreover, to support multiple-band systems and to increase the level of integration without increasing the chip area and thus the fabrication costs, multiple-band mm-Wave VCOs are highly desired. However, existing multiple-band VCO techniques, including tapped-inductor based [1] and transformer-based [2], are not suitable for mm-Wave frequency bands. Prediction of their performance is difficult due to the inaccurate modeling of both passive and active devices at the mm-Wave frequencies. In addition, the performance of these existing VCOs is typically not good because of the low quality factor of inductors and transformers. Wave-based oscillators such as standing-wave oscillators (SWO) can reach operation frequencies approaching the devices' transition frequency f_T with proper distribution of active gain elements along a transmission line. Given the quasi-transverse electromagnetic mode of propagation, transmission lines are capable of realizing precise values of small reactance and are inherently scalable in length. Also,

the well-defined ground return path significantly reduces magnetic and electric field coupling to adjacent structures [3].

In this work, a dual-band mm-Wave SWO at 24 GHz and 60 GHz is demonstrated by exploiting and switching the intrinsic multiple standing-wave modes. Employing only one differential transmission line, this dual-band VCO occupies an area of only 0.05mm^2 and achieves figures of merit (FOMs) in the two frequency bands comparable with that of existing single-band mm-Wave VCOs.

6.2 Multiple-Mode Oscillation of SWO

In a λ/4 SWO, the boundary conditions allow several standing-wave modes at l_0= λ/4×n (n=1, 3, 5 …) where l_0 is the length of transmission line. The corresponding frequency can be expressed as:

$$f_n \approx \frac{n}{4l_0\sqrt{LC}} \quad , \tag{6.1}$$

where L and C are the inductance and capacitance per unit length.

In the fundamental mode (n=1), the voltage amplitude exhibits monotonic variations as a function of the position with an oscillation frequency f_L as depicted in Fig. 6.1 (a). On the other hand, in the third-order mode (n=3), the voltage amplitude exhibits periodic variations along the transmission line with an oscillation frequency f_H as shown in Fig. 6.1 (b). Oscillations in the fifth mode and higher modes are insignificant and negligible due to the substantial high-frequency loss.

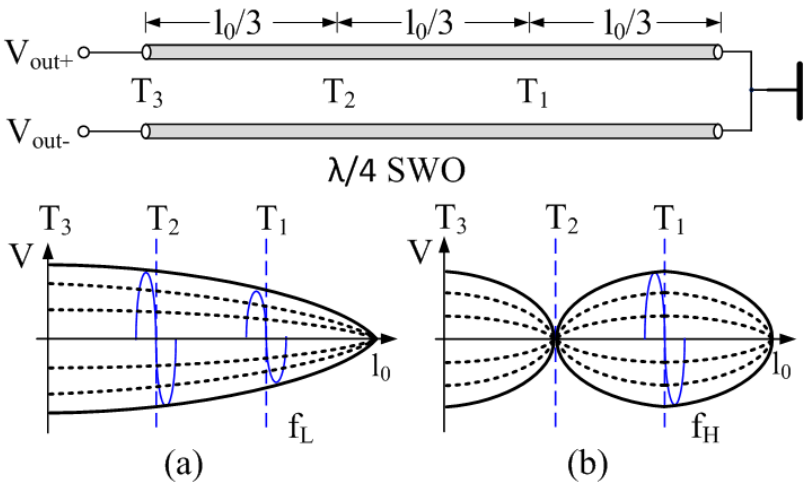

Fig. 6.1 Voltage amplitudes of a λ/4 SWO operating in (a) the fundamental mode and (b) the third-order mode

The multiple modes of SWO imply multiple impedance peaks of the transmission line. Using the S-parameters of the transmission line obtained from EM simulations in ADS Momentum and the capacitor models from the foundry, the small-signal model is built and simulated as shown in Fig. 6.2, where C_p is the parasitic capacitance. The impedance seen from Node T_3 exhibits two distinctive peaks with $|Z_{3L}| > |Z_{3H}|$, while the impedance seen from Node T_1 also exhibits two distinctive peaks: $|Z_{1H}| > |Z_{1L}|$, where $f_H \approx 3f_L$. As a result, mode-switching for dual-band operation can be achieved by injecting energy at different nodes, i.e. low-band and high-band oscillations are excited by injecting energy at Nodes T_3 and T_1, respectively.

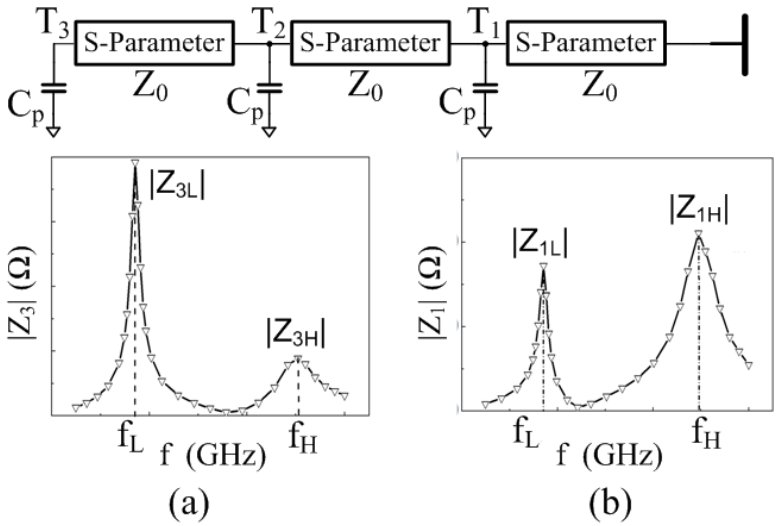

Fig. 6.2 Impedance seen at Nodes (a) T_3 and (b) T_1

6.3 Analysis on the Stability Issue

In order to achieve stable oscillation of the VCO, it is critical to ensure that the impedance at the desired frequency is significantly larger than that at the other frequencies. If energy is injected at Node T_3, the low-band oscillation is excited and can work stably since $|Z_{3L}|$ is much larger than $|Z_{3H}|$ as shown in Fig. 6.2 (a). However, if energy is injected at Node T_1, the high-band oscillation is potentially unstable and may jump to the low-band in the presence of process variations since $|Z_{1H}|$ is just slightly larger than $|Z_{1L}|$ as shown in Fig. 6.2 (b). Therefore, a stabilization technique is indispensable to achieve stable and proper oscillation.

Analysis on SWO is performed with transmission line theory in the situation when the high-band oscillation is desired by injecting energy at Node T_1. To simplify the calculation, it is assumed that parasitic capacitance is absorbed into the transmission line. By treating the SWO as a distributed oscillator, the start-up requirement can be

derived. Fig. 6.3 shows a simplified model of the SWO [4] with a negative-conductance stage injecting energy to Node T_1.

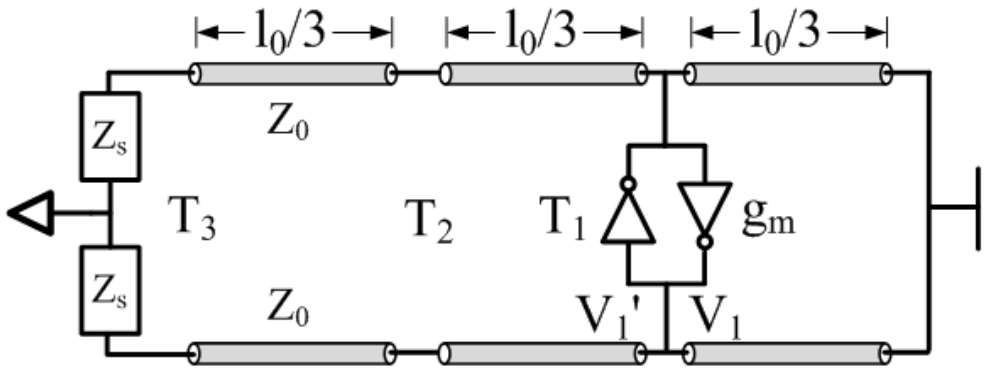

Fig. 6.3 Simplified model of SWO operating in the high-band mode

Starting from Node T_1, the forward wave V_1 is amplified by the gain stage and travels toward the right end where it is completely reflected. The first reflected wave travels along the transmission line to the left until it arrives at Node T_3 where it is partially reflected if Z_s is neither infinitely large nor 0. The second reflected wave propagates along the transmission line to the right and finally reaches T_1 where it is amplified to V_1'. The amplitude of V_1' can be expressed as:

$$V_1' = -\left(\frac{1}{2} g_m Z_0\right)^2 e^{-(\alpha + j\beta)2l_0} \Gamma_3 V_1 \quad , \tag{6.2}$$

where α is the attenuation constant and β is the phase constant of the transmission line. The reflection coefficient at Node T_3 can be express as:

$$\Gamma_3 = |\Gamma_3| e^{j\theta} = \frac{Z_s - Z_0}{Z_s + Z_0} = 1 - \frac{2Z_0}{Z_s + Z_0} \quad . \tag{6.3}$$

To satisfy the phase condition for oscillation:

$$e^{-j\beta \cdot 2l_0} e^{j\theta} = -1 \quad , \tag{6.4}$$

The required normalized gain to sustain oscillation can be derived by setting $|V_1|= |V_1'|$, that is:

$$\left(\frac{1}{2} g_m Z_0\right)^2 = \frac{1}{e^{-\alpha \cdot 2l_0} \left|\Gamma_3\right|} \ . \tag{6.5}$$

As the attenuation α increases with frequency, the high-band oscillation would need more energy than the low-band oscillation. However, the gain condition is relaxed and the high-band oscillation is easily achieved if $|\Gamma_3|$ is increased with frequency, which can be implemented by adding capacitor C_s at Node T_3 in such a way that $C_s > l0C$, where C is the capacitance per unit length. This result is further verified by simulation. As shown in Fig. 6.4 (b), the difference between $|Z_{1L}'|$ and $|Z_{1H}'|$ becomes more distinct if C_s is added. However, since C_s is in parallel with the transmission line, $|Z_{3L}|$ decreases to $|Z_{3L}'|$ as shown in Fig. 6.4 (a), and thus more power is needed to sustain the low-band oscillation. The oscillation frequencies f_L and f_H are also shifted down due to the loading effect of C_s.

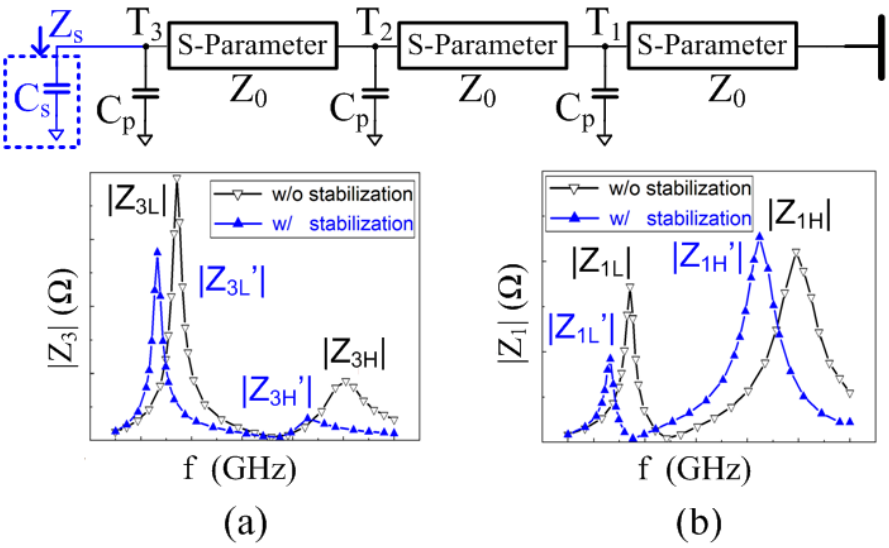

Fig. 6.4 Impedance with and without stabilization technique seen at Nodes (a) T_3 and (b) T_1

The mode-switching SWO can also be approximated by a lumped model which is simply a second-order LC tank. After calculating the impedance seen from Nodes T_1 and T_3 and utilizing the notch-peak cancellation concept [2], it can be proved that adding capacitance at Node T_3 can help suppress unwanted oscillation and hence stabilize desired oscillation, which is consistent with the results from the analysis above with a distributed model.

6.4 Circuit Design and Implementation

Fig. 6.5 shows the schematic of the proposed dual-band standing-wave VCO with the stabilization technique. The differential transmission line is implemented by a differential micro-strip line with the topmost and thickest Metal 8 as the signal line and Metal 1 as the ground plane. The width is optimized to be 16 μm to maximize the quality factor Q at the frequency in the middle of the range. Frequency tuning is done by two varactors C_{v1} (~40fF) and C_{v3} (~300fF) located at Node T_1 and Node T_3, respectively. Large C_{v3} is used to ensure no frequency jumping while small C_{v1} and no varactor at Node T_2 are employed to reduce the effective loading capacitance at Node T_1. Three equally-spaced NMOS cross-coupled negative g_m cells g_{m1}, g_{m2}, and g_{m3}, with an additional g_{m1}' at Node T_1 are utilized to compensate the losses of the transmission lines and varactors. Each of the g_m cells is a current-biased g_m cell which can be fully turned on/off by switching the bias current. Series switches are avoided in the high-frequency signal path to minimize attenuation. In the presence of the capacitance contributed from varactors and parasitics, the length of the transmission line is chosen to be 260 μm to obtain the desired output frequency.

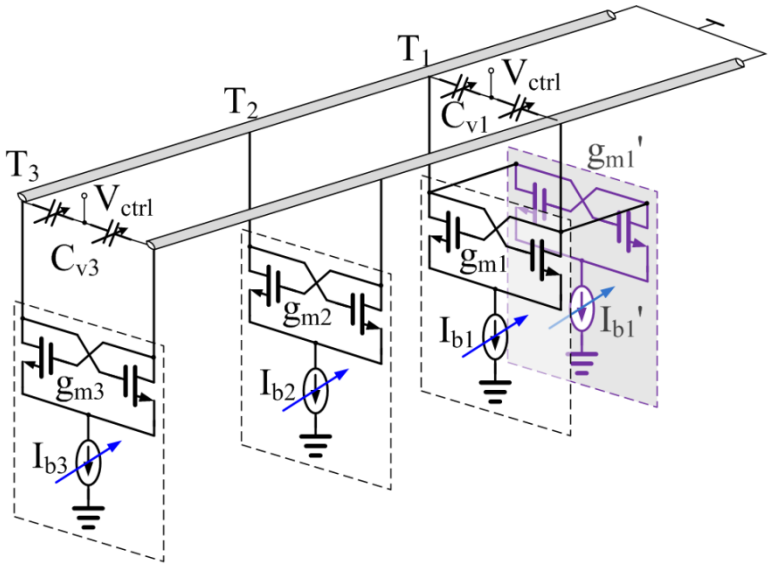

Fig. 6.5 Proposed dual-band standing-wave VCO

Dual-band operation is achieved by switching different combinations of negative gm cells at different nodes. When g_{m1}, g_{m2}, and g_{m3} are activated by turning on their associated bias currents I_{b1}, I_{b2}, and I_{b3}, energy is injected to all the three nodes T_1, T_2, and T_3. As a result, the fundamental-mode standing-wave is excited, and the low-band oscillation is obtained. In this mode, the three negative gm cells are distributed to reduce the effective parasitic capacitance at the output. They are also scaled to be $g_{m3} = 2g_{m2} = 2g_{m1}$ to save the power consumption [4]. On the other hand, when g_{m1} and g_{m1}' are activated by turning on the bias currents I_{b1} and I_{b1}', energy is only injected to Node T_1. As such, the third-mode standing-wave is excited, and the high-band oscillation is obtained. The loading capacitance at Node T_3 looks smaller at Node T_1 due to the loss of the transmission line [5], but the impedance is still low that both g_{m1} and g_{m1}' are needed for high-band oscillation.

6.5 Experimental Results

A dual-band standing-wave VCO prototype operating at 24 GHz and 60 GHz in a 0.13μm CMOS process is implemented with proposed stabilization technique. The core area occupied is 0.31×0.16 mm^2, as shown in Fig. 6.6.

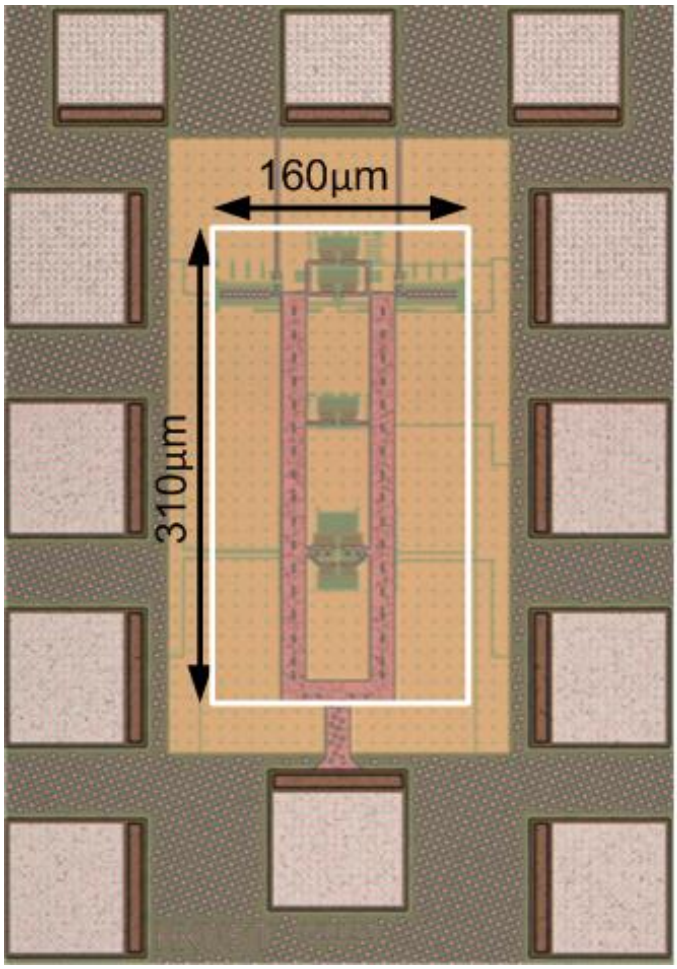

Fig. 6.6 Chip photograph of proposed dual-band VCO

6.5.1 Measured Frequency Tuning Curves

With 0.8V and 1.2V supply voltages, the frequency tuning curves are measured as shown in Fig. 6.7.

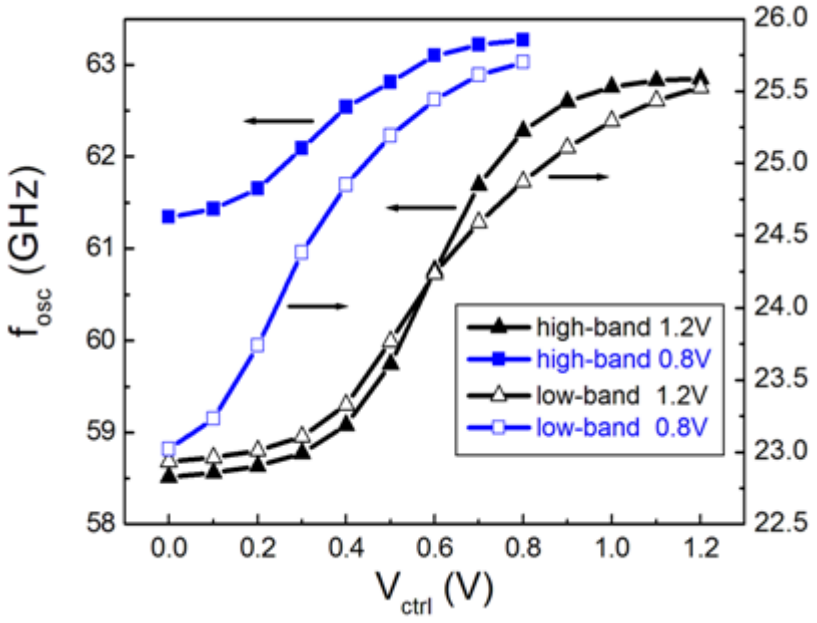

Fig. 6.7 Measured frequency tuning curves with 0.8V and 1.2V supply voltages

6.5.2 Measured Phase Noise

For low-band phase noise measurement, the output is measured directly with Agilent E4440A spectrum analyzer, and the phase noise is -120dBc/Hz at 10MHz offset while drawing a current of 14mA from a 0.8V supply, as shown in Fig. 6.8.

For high-band phase noise measurement, the output signal is first down-converted by Ducommun V-band balanced mixer with LO input at 50 GHz and then measured with spectrum analyzer. With current consumption of 20mA from a 1.2V supply, the phase noise is -114dBc/Hz at 10MHz offset, as shown in Fig. 6.9.

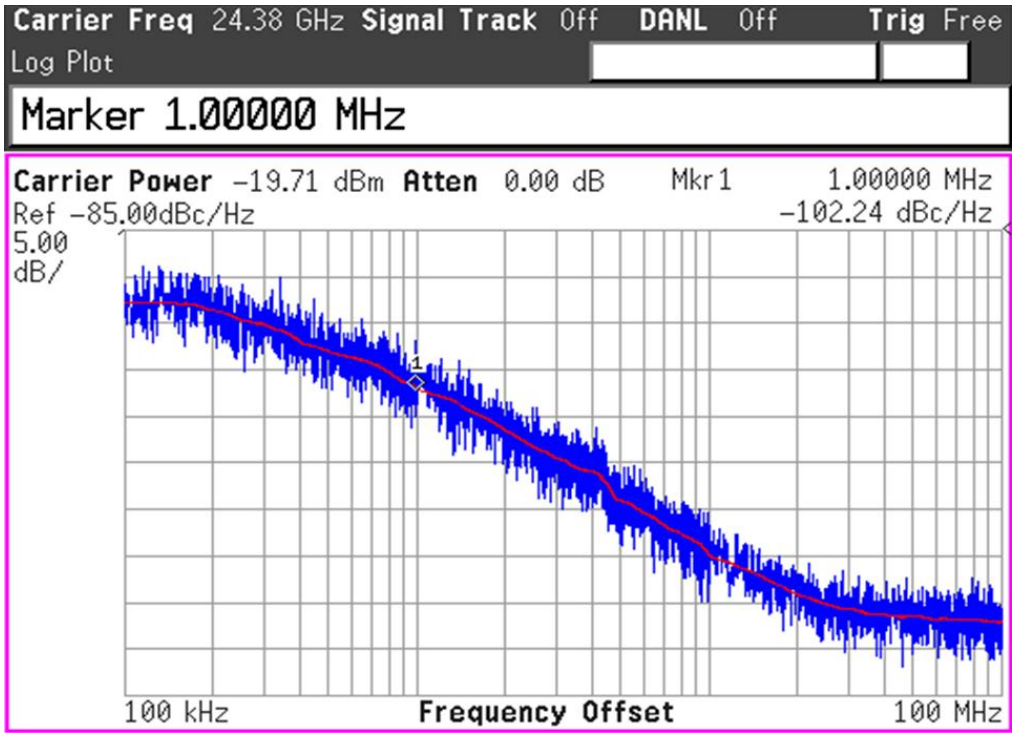

Fig. 6.8 Measured phase noise in low-band mode at 24GHz

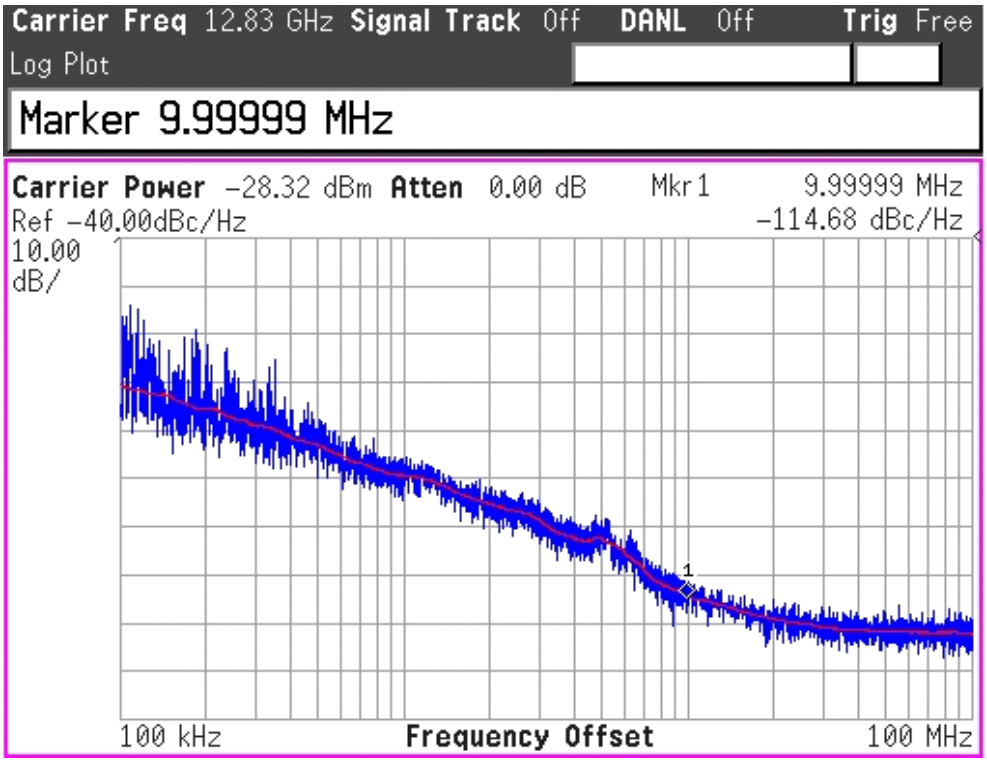

Fig. 6.9 Measured phase noise in high-band mode at 60GHz

6.5.3 Performance Summary

The performance and comparison with recent published state-of-art dual-band VCOs and mm-Wave VCOs are summarized in Table 6.1.

Table 6.1 Performance summary and comparison

Ref.	This Work		[2]		[4]	[5]	[6]
Technology	0.13 μm CMOS		0.18 μm CMOS		0.18 μm CMOS	90 nm CMOS	90 nm CMOS
f_{osc} [GHz]	24	60	4.2	10	40	75	58.4
FTR	10.80%	7.20%	42.00%	18.00%	20.00%	1.30%	9.32%
PN [dBc/Hz]	-120@10M	-114@10M	-116@1M	-112@1M	-100@1M	-108@10M	-91@1M
Supply [V]	0.8	1.2	1.0	1.0	1.5	1.45	0.7
P_{diss} [mW]	11	24	6	10	27	8	8.1
FoM [dB]	-177	-176	-181	-182	-178	-176	-177

6.6 Conclusion

In this work, a mm-Wave mode-switching technique with standing-wave architecture is presented. Based on the detailed stability analysis with a distributed model, a stabilization technique is proposed and demonstrated for a dual-band mm-Wave VCO with good performance. The oscillation frequencies are much higher than existing dual-band VCOs while the performance is comparable to existing single-band mm-Wave VCOs.

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Chapter 7

LO Generation with Automatic Phase Tuning

7.1 Introduction

High-date-rate wireless communication is highly desired for many emerging mass-market applications such as high-definition video links and wireless personal area networks. The required wide bandwidth has driven the operation frequency of RF transceivers move from several-GHz range up to millimeter-wave (mm-Wave) region. At mm-Wave frequencies, the free space loss is typically large that the link budget of the transceiver is very stringent.

Conventionally, III/V compound semiconductor technology is employed due to its best overall performance for mm-wave ICs (MMICs) [1] in terms of unity current gain frequency f_T and the output power of power amplifier, but the cost is too high for most of the commercial products to afford. As the feature size aggressively scaled down to nanometer, today's advanced CMOS technology is applicable for the implementation of MMICs. With high yield and high integration level, CMOS technology leads to a lower cost and more compact solution, by integrating the RF and analog circuits as well as the digital signal processing and baseband circuits in the lowest possible chip area. However, several challenges must be overcome, such as low output power and nonlinearity of power amplifiers, limited gain of the low noise amplifier and its high noise figure at mm-wave frequencies.

Phased-array is an excellent promising solution to address these challenges, because it imitates the behavior of high-gin directional antennas whose bearing can be adjusted electrically. More specifically, they can be used not only to combine the power spatially and thus relax the requirement of signal power of each element but also to electrically steer the beam direction to suppress the unwanted signals and thus increase the spectrum efficiency. In a phased-array, each element requires an adjustable time delay to compensate for the time difference between adjacent elements depending on the angle of the radiated or incident signal such that a maximum gain is achieved in that particular direction. For narrow band system, the adjustable time delay is often approximated with a phase shifter to ease the implementation [2], and hence both the spatial power combing and beamforming capabilities of a phased-array highly depend on the performance of the phase shifter. Its variable phase range determines the steerable beam direction range, and both the phase accuracy and amplitude variations affect the peak-to-null ratio of the system. To ease the control circuits design, the relationship between the control signal and output phase is desired to be linear. From the aspect of implementation, both the complexity and interference of signal routings should be reduced as much as possible. Lastly, the power consumption should be minimized.

Both passive and active phase shifters have been proposed for on-chip phased-array systems. Traditional passive types are mainly based on distributed transmission line networks [3]-[4] and thus quite area consuming. The migration from the distributed approaches to lump-element configurations, such as synthetic transmission lines with capacitors and inductors [5], and hybrid coupler with reflective loads [6]-[7] could reduce the physical dimension, but the multiple inductors needed still occupy a large

chip area. In addition, passive phase shifters suffer from some drawbacks such as the large insertion loss, output amplitude variations and nonlinear output phase shift versus control signal. On the other hand, most of the active phase shifters synthesize the phase shift by interpolating the phases of two input signals with orthogonal phases [8]-[11]. With power consumption, they feature small area and small insertion loss. However, the routing of the I/Q-phase input signals instead of differential input signals tends to introduce more phase error due to interference, especially at high frequencies. Besides, the amplitude weighting control of the I/Q-phase signals to generate specified phases within small amplitude variation is very complicated.

Conventionally, the phase shift is controlled by the baseband with exhaustive tuning algorithm, which elaborates all possible phase controls to get the best performance in terms of peak-to-null ratio for each phase difference between adjacent elements specified by the system. Therefore, the tuning time is very long and grows exponentially as the element number increases. A calibration signal can be fed to the phase shifter and hence the phase and amplitude characteristics of each phase shifter are measured and stored in a lookup table [6] to be selected by a baseband control algorithm as the beam direction changes. As such, the phase tuning time can be significantly reduced. Due to process variations, the characteristics of the phase shifters are different so that each sample needs its own lookup table. As a result, the total time for setting up the lookup tables would be long and the total cost would be high. Gradient estimation approach such as zero-knowledge beamforming algorithm can adjust the phase control on line, but the complicated calculation heavily burdens the baseband that a complex and power-hungry processor is needed [12].

This work presents a new 4-path LO generation scheme with automatic phase tuning for 60GHz phased-array receiver in 65nm CMOS technology. The proposed phase shift chain composed of phase shifter cascaded with frequency tripler features linear phase shift, small output amplitude variations, differential input/output and thus low power consumption. The phase shift of each path can be detected and tuned automatically with proposed successive-approximation algorithm.

The content is organized as follows. First, the building blocks of proposed LO phase shift generation system are introduced in Section 7.2. In Section 7.3, proposed successive-approximation algorithm is described and illustrated. In Section 7.4, design consideration and circuit implementation of critical building blocks are discussed. Finally, Section 7.5 presents the experimental results, and the conclusion is given in Section 7.6.

7.2 System Architecture

7.2.1 Phase Shifting Configuration

To steer the beam direction of the phase-array receiver, phase shifters can be incorporated in different stages. Hence, different phased-array configurations such as RF-path, LO-path and IF/baseband phase shifting have been developed. Low power consumption and small chip area motivate the selection of RF-path shifting [13]-[14], because of the least number of parallel building blocks required per element. But RF-path shifting results in the potential system performance degradation that the key requirements of insertion loss, noise figure, linearity and dynamic range are quite stringent. To the contrary, IF/baseband phase shifting [15] lowers the operation

frequency of the phase shifters and thus ease their design and implementation with the penalty of the largest number of hardware used. LO-path phase shifting [9] [11] is advantageous since the circuits in the LO path operate in saturation and the system performance in relatively insensitive to LO amplitude difference corresponding to different phase shifts. Therefore, LO-path phase shifting is a proper candidate for phase shift generation in an mm-wave phased-array with smaller element number.

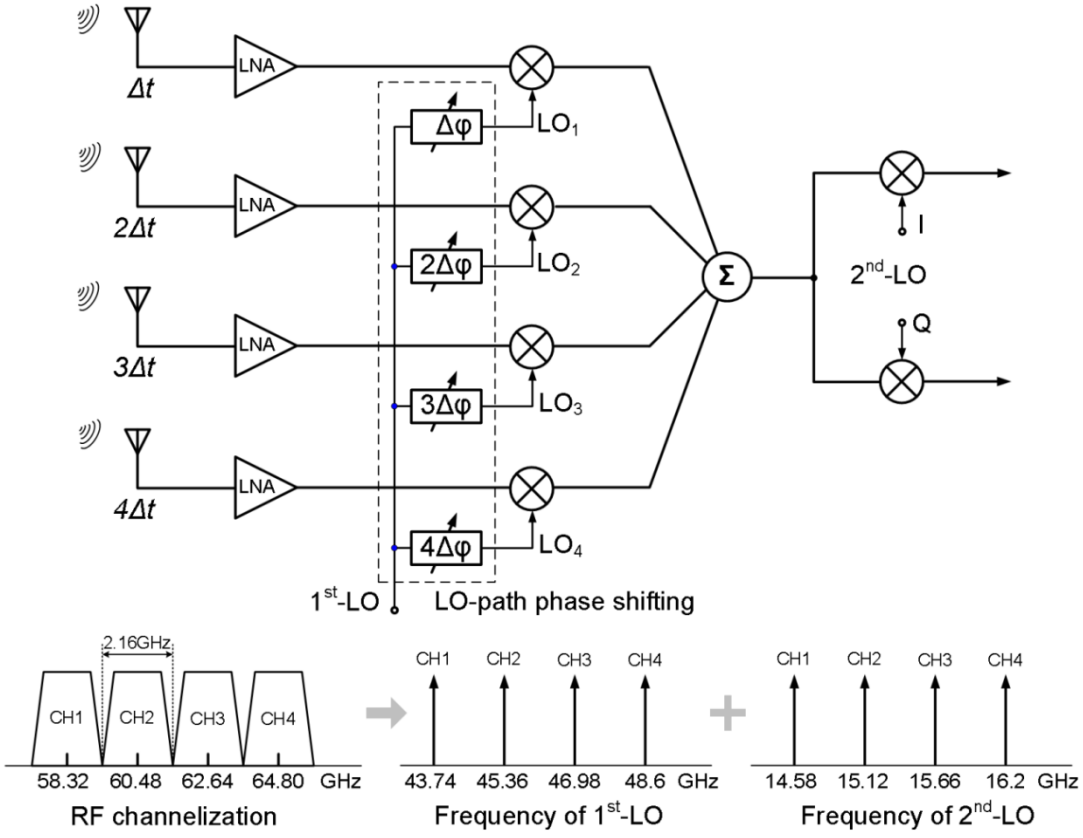

Fig. 7.1 Phased-array receiver architecture with LO-path phase shifting

The proposed LO generation scheme with phase shifting is designed for a 4-element 60GHz phased-array receiver with dual-conversion zero-IF architecture according to the IEEE 802.15.3c standard [16]. The frequency of the first LO is designed to be three times as high as that of the second LO. Therefore, the first LO is

located at 43.74 / 45.36 / 46.98 / 48.6 GHz while the second LO is at 14.58 / 15.12 / 15.66 / 16.2 GHz corresponding to CH1 / CH2 / CH3 / CH4 centered at 58.32 / 60.48 / 62.64 / 64.80 GHz, respectively. As shown in Fig. 7.1, to substantially relax the requirement of the phase shifters in terms of linearity, noise figure, and bandwidth, the phase shifts are implemented in the first LO path: the progressive variable phase shift $\Delta\varphi$ compensates the time difference Δt between adjacent elements depending on the angle of incident signals.

7.2.2 Proposed Variable Linear-Phase-Shift Chain

When an oscillator is injection-locked by the input signal, its output frequency equals to the input frequency, and the phase difference between input and output can be tuned by changing its self-oscillation frequency. Therefore, injection locking could be utilized to generate variable phase shift [17]. Approximately, the relationship between the phase shift and the self-oscillation frequency is an arcsine function [18]:

$$\Delta\varphi_{ps} = sin^{-1}\left(\frac{f_o - f_{in}}{f_L}\right) \tag{7.1}$$

where $\Delta\varphi_{ps}$ is the phase shift between output and input, f_{in}, f_o and f_L are input frequency, self-oscillation frequency and locking range, respectively.

As plotted in Fig. 7.2 (a), the phase shift is non-linear outside the range of ±30°, which would not only make the control circuit complicated but also limit the achievable minimum phase error. Fortunately, within the range from -30° to 30°, the phase shift is linear, which is highly desired for the phased-array.

This work proposes a variable phase shift generation chain which is composed of an injection-locked oscillator based phase shifter cascaded with an injection-locked

frequency tripler, as shown in Fig. 7.2 (b). The frequency tripler not only triples the frequency, but also triples the phase shift. Therefore, the phase shifter only needs to operate at 1/3 of the output frequency and to linearly tune from -30° to 30° to achieve an effective linear phase range from -90° to 90° at the tripler's output. This small range helps eliminate the problems with nonlinearity and too high sensitivity to control signals in the existing injection-locked phase shifters that have to make use of the whole range. In addition, the injection-locked tripler is insensitive to the input amplitude mismatches since its output amplitude is dominated by its self-oscillation current and voltage swing. So a major drawback of conventional phase shifters that their gain varies with phase shift settings resulting in amplitude mismatches over the phase range [19] doesn't exists. Overall, the proposed phase shift chain has a very linear phase shift range from -90° to 90° with very small amplitude variations. Furthermore, a full linear phase range from -180° to 180° for the system can be simply obtained by flipping the outputs.

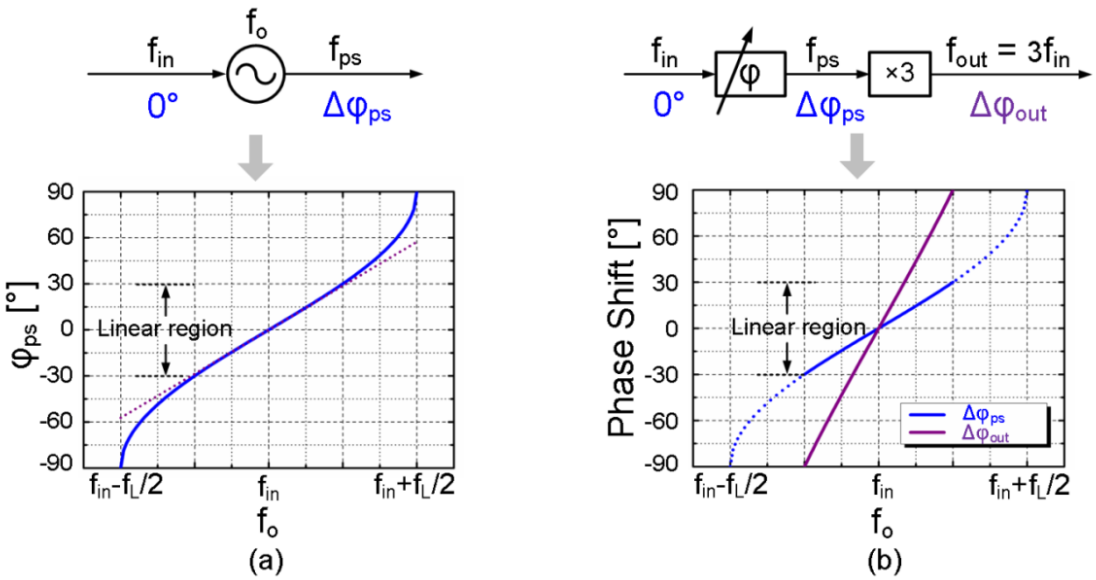

Fig. 7.2 (a) Injection-locked oscillator based phase shifter, (b) Proposed linear-phase-shift generation chain

7.2.3 Proposed LO Generation System

With proposed variable linear-phase-shift chain, a 4-path LO generation scheme for 60-GHz phased-array receiver is constructed and the block diagram is depicted in Fig. 7.3. The off-chip single-ended LO input at 14.58 / 15.12 / 15.66 / 16.2 GHz is symmetrically routed to the inputs of 4 on-chip baluns and converted to differential at their outputs. With each of the balun driving one path, the phase errors of the differential LO for each path depend solely on their respective baluns. As the differential signals pass through their respective phase shifter, a phase shift of $\varphi_{1\text{-}4}$ is introduced depending on the control signals $D_{ctrl1\text{-}4}$ and $V_{ctrl1\text{-}4}$, which are for digitally coarse tuning and analog fine tuning, respectively. The signals are then fed into injection-locked frequency triplers, through which both their frequencies and phases are tripled. 2-stage buffers are then employed to increase driving capability of each path.

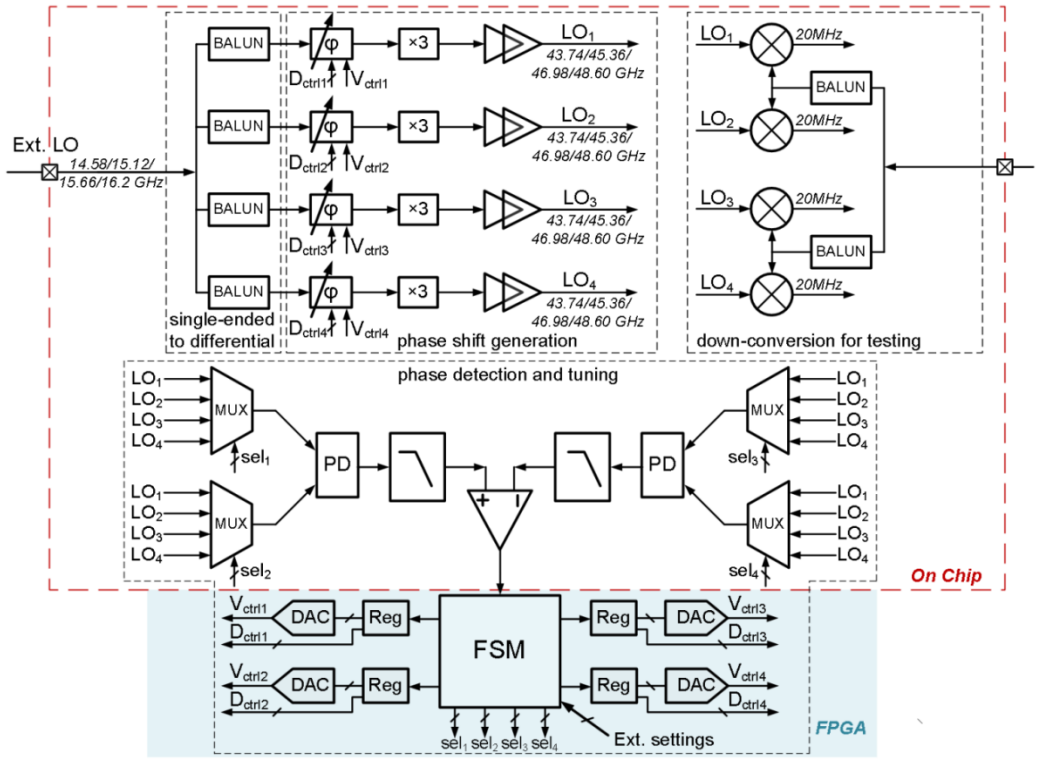

Fig. 7.3 Block diagram of proposed LO generation scheme with automatic phase tuning

To measure the phases accurately, the 4-path outputs are down-converted to 20MHz with 4 on-chip mixers so that time-domain measurement can be performed with an oscilloscope. The down-conversion mixers are divided into two groups, each of which is driven by a balun that converts the external single-ended signal to differential.

Furthermore, the 4-paths outputs are used to drive on-chip phase detection followed by off-chip control-signal generation to form a closed-loop system for automatic phase tuning. The on-chip part is composed of two phase detectors with low-pass filters and an error amplifier. Driven by a multiplex (MUX), each input of the phase detector can be configured to be either one of the 4-path LO outputs. The off-chip part implemented with an FPGA development board consists of a finite-state machine (FSM) followed by registers (Regs) and digital-to-analog converters (DACs). Registers are used to set the digital controls such as coarse-tuned $Dctrl_{1\text{-}4}$ of phase shifters and $sel_{1\text{-}4}$ of MUXs, while the DACs convert the digital control signal from FSM to analog for the fine-tuned $Vctrl_{1\text{-}4}$ of phase shifters. In this closed-loop system, the FSM can select the desired signals for detection and tune the phase shifter automatically according to the proposed successive-approximation algorithm.

7.3 Automatic Phase Tuning

7.3.1 Successive-Approximation Algorithm

Directly measuring a phase difference is quite difficult, especially for high frequency signals. Instead, the phase difference is typically converted to voltage by a phase detector which is implemented by an analog mixer or multiplier, as shown in Fig. 7.4 (a).

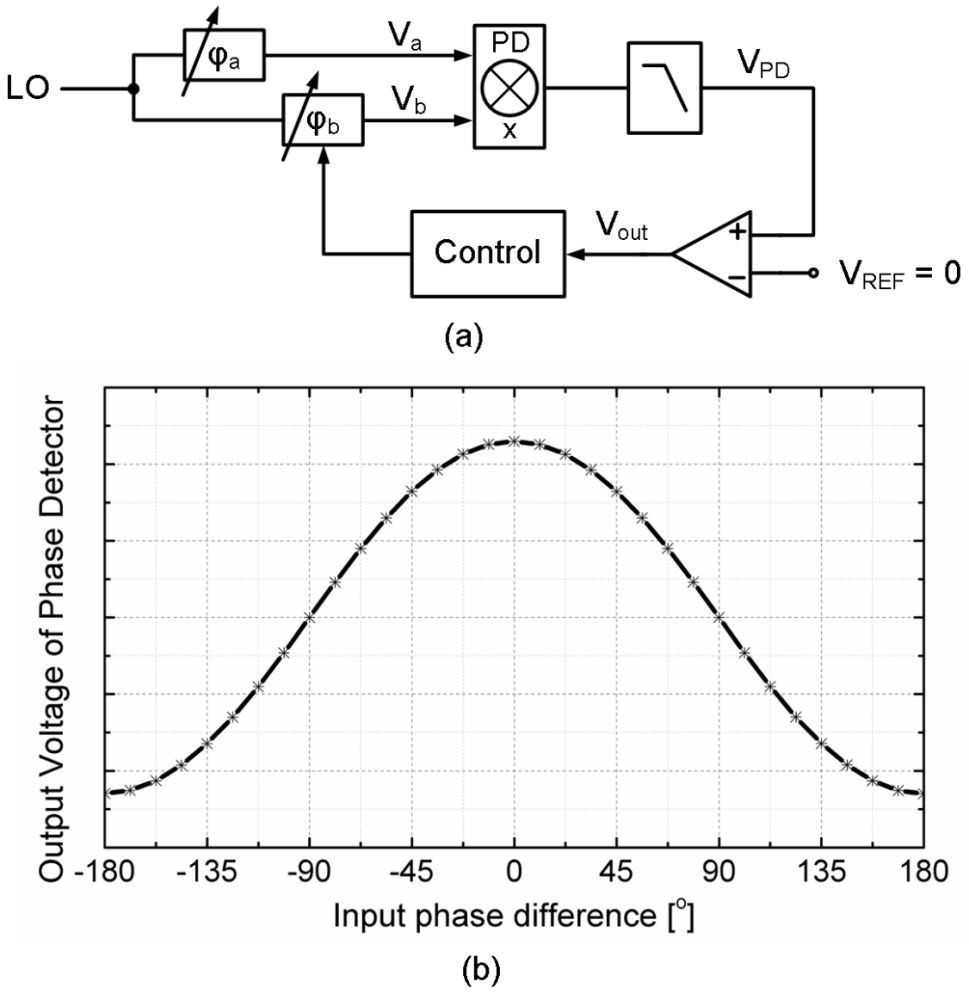

Fig. 7.4 I/Q calibration: (a) phase detection and tuning loop, (b) input/output characteristic of phase detector

Assuming each of the two inputs is a cosine wave with the same frequency and amplitude but with independent phase, as shown below:

$$V_a = V \cdot cos(\omega t + \varphi_a) \ , \tag{7.2}$$

$$V_b = V \cdot cos(\omega t + \varphi_b) \ . \tag{7.3}$$

Due to the mixing, the output of the phase detector is derived as:

$$V_a \cdot V_b = \frac{1}{2}V^2 \cdot cos(\varphi_a - \varphi_b) + \frac{1}{2}V^2 \cdot cos(2\omega t + \varphi_a + \varphi_b) \ . \tag{7.4}$$

Low-pass filter rejects the high-frequency component and keep the DC component:

$$V_{PD} = \frac{1}{2}V^2 \cdot cos(\varphi_a - \varphi_b) \ , \tag{7.5}$$

which indicates that the output voltage of the phase detection is a cosine function of the input phase difference, as plotted in Fig. 7.4 (b). The absolute voltage $|V_{PD}|$ reaches the maximum and minimum point when the phase difference is 0/180° and ±90°, respectively. Therefore, I/Q calibration [20]-[21] can be implemented by a simple close-loop shown in Fig. 7.4(a). By setting the reference voltage V_{REF} to be 0 and tuning the phases of the input signals until the voltage of phase detection $|V_{PD}|$ equals to V_{REF} and thus the output of error amplifier is 0, a ±90° phase difference is achieved. However, the I/Q calibration loop is not suitable for detecting and calibrating the phase difference other than ±90°, because directly generating a specified reference voltage corresponding to that phase difference is really difficult.

Fortunately, this required reference voltage can be provided by another phase detector whose inputs are V_c and V_d with respective phase of φ_c and φ_d, as shown below:

$$V_{REF} = \frac{1}{2}V^2 \cdot cos(\varphi_c - \varphi_d) \ . \tag{7.6}$$

By tuning the phases and thus making $|V_{PD}|$ the same as $|V_{REF}|$, $(\varphi_a - \varphi_b)$ is equal to $(\varphi_c - \varphi_d)$. Furthermore, a phase of $\varphi_b = (\varphi_a + \varphi_d)/2$ can be obtained if both φ_a and φ_d are known and $\varphi_b = \varphi_c$. This is the key idea of proposed successive-approximation algorithm, whose implementation is shown in Fig. 7.5 (a). V_a and V_b, V_c and V_d are inputs to phase detectors (PDs) x and y, respectively. With MUXs, each of them can be configured to be any output of the 4-paths, i.e. $LO_{1\text{-}4}$. After the phase detectors with low-pass filters, the DC signals V_x and V_y are proportional to the cosine of the difference of the input phases. The comparator's inputs, V_+ and V–, can then be selected

to be either V_x, V_y or 0.

Starting from I/Q calibration, any phase of $90°/2^k$ can be obtained by successively detecting and tuning $90°/2^i$, with i starting from 0, 1, ⋯, k. An example of achieving a 22.5° difference between neighboring paths is illustrated in Fig. 7.5 (b). The first step is to obtain $\Delta 90° = \angle LO_4 - \angle LO_1$. Similar to the traditional IQ calibration, $\angle LO_1$ is used as a 0° reference while $\angle LO_4$ is tuned until $V_x = 0$. In Step II, both $\angle LO_1$ and $\angle LO_4$ are now used as references such that V_+ and V_- are configured to be proportional to $\cos(\angle LO_3 - 0°)$ and $\cos(90° - \angle LO_3)$ respectively. By tuning $\angle LO_3$ until $V_+ = V_-$, $\angle LO_3$ is set to 45°. After two more similar steps, $\angle LO_1$, $\angle LO_2$, $\angle LO_3$, and $\angle LO_4$ can be tuned to be 0°, 22.5°, 45°, and 67.5°, respectively.

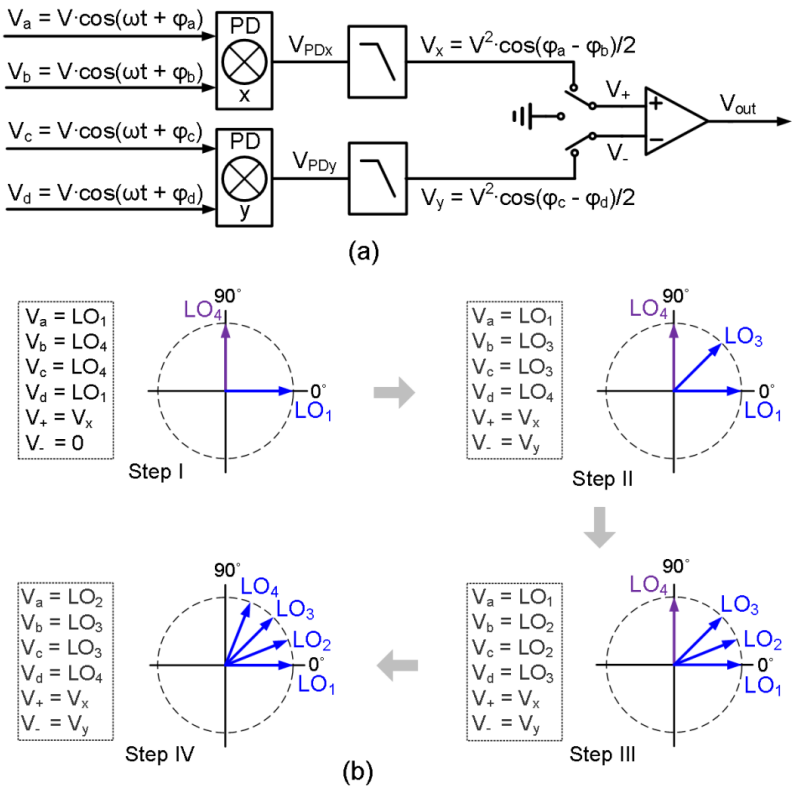

Fig. 7.5 Proposed successive-approximation algorithm: (a) block diagram, (b) automatic phase tuning of Δ22.5°

7.3.2 Port Swapping and Averaging

Theoretically, any phase of $90°/2^k$ can be tuned. However, in reality, mismatches and offset errors in the phase detectors limit the minimum detectable phase. To simplify the analysis, the equivalent phase error is modeled at the inputs as two parts, phase independent part and phase dependent part, as shown in Fig. 7.6 (a). With V_a and V_b respectively feeding Port 1 and Port 2 of the phase detector, the output voltage is written as:

$$V_{PD} = \frac{1}{2}V^2 \cdot cos[\varphi_a - \varphi_b - (\theta_i + \theta_d)] \ , \tag{7.7}$$

where θ_i and θ_d are phase independent part and phase dependent part of equivalent input phase error.

For I/Q calibration,

$$V_{PD} = 0 \ \rightarrow \ \varphi_a - \varphi_b - (\theta_i + \theta_d) = \pm 90° \ . \tag{7.8}$$

By swapping the ports, as shown in Fig. 7.6 (b), which means Port 1 and Port 2 are fed with V_b and V_a respectively, it can be derived as:

$$V'_{PD} = 0 \ \rightarrow \ \varphi_a - \varphi_b + (\theta_i' + \theta'_d) = \pm 90° \ . \tag{7.9}$$

Since $\theta_i = \theta_i'$ and $\theta_d \neq \theta_d'$, by averaging the control signals and thus the phase, the phase difference becomes as:

$$\varphi_a - \varphi_b - \frac{1}{2}(\theta_d - \theta'_d) = \pm 90° \ . \tag{7.10}$$

The above equation shows that the phase independent part is completely cancelled and thus the phase error gets reduced, assuming the phase dependent part is not dominant.

Monte-Carlo simulations have been performed to show the phase error. By setting 3σ-mismatches of the devices, the results of 90° phase detection plotted in Fig. 7.6 (c)

show that the standard phase deviation σ and maximum phase error without port swapping are 1.5° and 4.4°, which is reduced to 0.3° and 0.91° with port swapping and averaging, respectively.

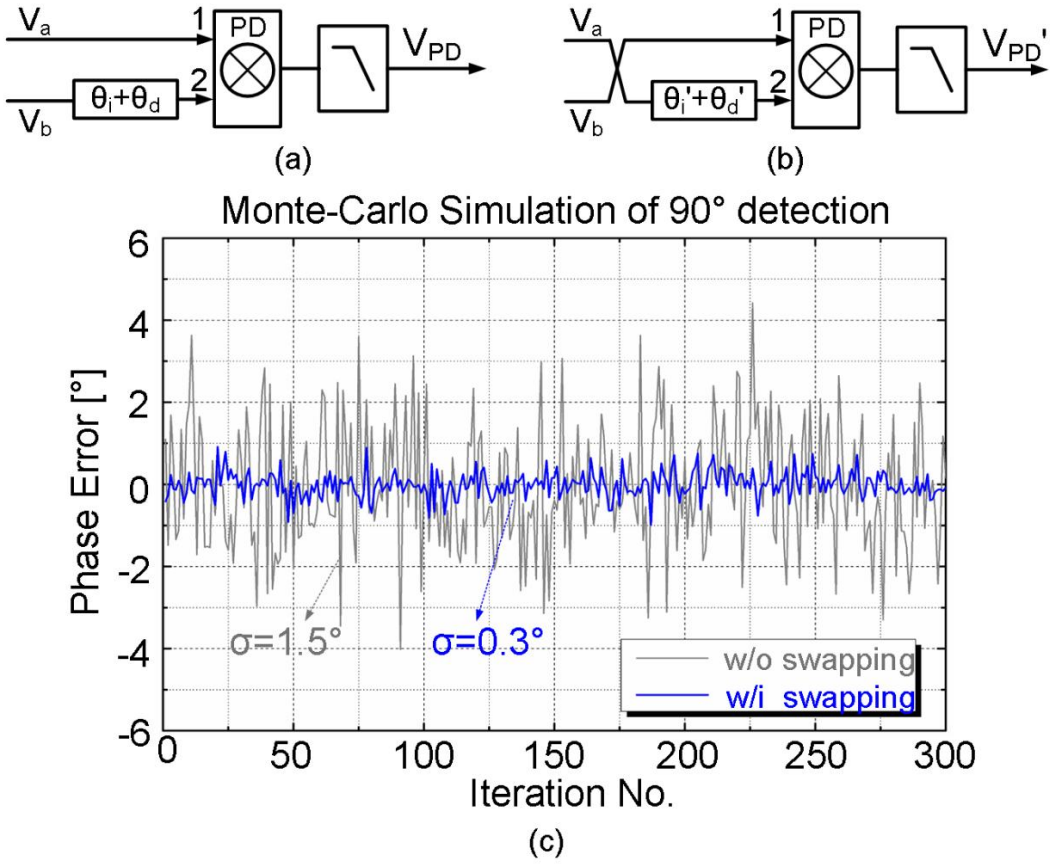

Fig. 7.6 Proposed port swapping and averaging: (a) input sequence without swapping, (b) input sequence with swapping, (c) Monte-Carlo simulation results

7.4 Circuit Design and Implementation

7.4.1 Phase Shifter

The phase shifter is based on injection-locked oscillator and the schematic is shown in Fig. 7.7. There are two branches of active devices, self-oscillation and injection. The

former is composed of tail current I_{osc} and cross-coupled transistors $M_{1,2}$ implementing the negative transconductance, and the latter is composed of tail current I_{inj} and differential pairs $M_{3,4}$ realizing the injection transconductance. To save power consumption but still have enough frequency locking range, the injection branch is sized to be 1/2 of self-oscillation branch. The input frequency f_{in} is typically in vicinity of the resonant frequency f_o of LC tank:

$$f_o = (1+\alpha) f_{in} \ , \tag{7.11}$$

where α is small. Assuming the input and output voltage swings are large enough that the transistors $M_{1\text{-}4}$ are hard-switching, the locking range f_L can be approximated [18] as:

$$f_L = \frac{f_o}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \ , \tag{7.12}$$

Therefore, the phase shift can be derived from Eq. (7.1), (7.11) and (7.12) as:

$$\Delta\varphi_{ps} = sin^{-1}\left(\frac{\alpha}{1+\alpha} \cdot 2Q \cdot \frac{I_{osc}}{I_{inj}} \cdot \sqrt{1-\left(\frac{I_{osc}}{I_{inj}}\right)^2}\right) \ , \tag{7.13}$$

As long as α is small, the above equation can be further simplified by approximation:

$$\Delta\varphi_{ps} = sin^{-1}\left(\alpha \cdot 2Q \cdot \frac{I_{osc}}{I_{inj}} \cdot \sqrt{1-\left(\frac{I_{osc}}{I_{inj}}\right)^2}\right) \ , \tag{7.14}$$

For the LC tank, the inductance is implemented by a differential coil with a center tap to save area and improve quality factor, while 7-bit switched-capacitor arrays (SCAs) and varactors are used for digital coarse tuning and analog fine tuning of the self-oscillation frequency. To implement a 7-bit SCA, traditionally 127 unit capacitors are needed

which would make the layout very complicated and introduce significant parasitic capacitance. Therefore, to simplify the layout by reducing the number of capacitors, the 7-bit SCA is divided into two groups from b_0 to b_3 and b_4 to b_6 with unit capacitance of $C_{unit\text{-}L}$ and $C_{unit\text{-}H}$, respectively. $C_{unit\text{-}L}$ is sized slightly larger than 1/16 times $C_{unit\text{-}H}$ to ensure a continuous resonant frequency range and thus guarantee the phase overlapping.

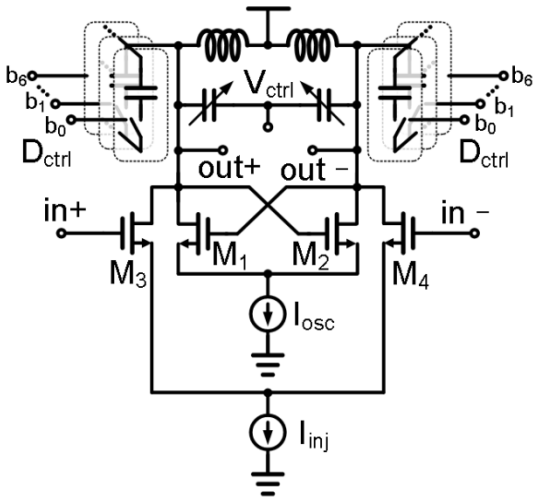

Fig. 7.7 Phase shifter based on injection-locked oscillator

7.4.2 Injection-Locked Frequency Tripler (ILFT)

Injection-locked frequency tripler features high operation frequency and low power consumption, but the locking range is very limited. Fig. 7.8 (a) shows the schematic of a conventional injection-locked frequency tripler, which can be modeled as a feedback loop composed of a band-pass filter (BPF) composed of LC tank and two single-balanced mixers, as shown in Fig. 7.8 (b). At the output, due to the filtering of the BPF, only the third-order harmonic tone $v_{o,3\omega}$ at a frequency in vicinity of the LC tank's resonant frequency ω_o exists and is fed back to a mixer and mixed with the DC current I_{osc} of self-oscillation, resulting in a current of $i_{o,3\omega|(I_{osc}*v_{o,3\omega})}$. The other mixer performs

harmonic mixing of I_{dc} with the input voltage $v_{inj,\omega}$ due to the nonlinearity of the switching devices, and produces an output current of $i_{o,3\omega|(I_{dc}*v_{inj,3\omega})}$. These two branches of current injected to the LC tank can be written as:

$$i_{o,3\omega|(I_{osc}*v_{o,3\omega})} = k_{3\omega|(I_{osc}*v_{o,3\omega})} \cdot I_{osc} \cdot cos(3\omega t + \theta) \ , \qquad (7.15)$$

and

$$i_{o,3\omega|(I_{dc}*v_{inj,3\omega})} = k_{3\omega|(I_{dc}*v_{inj,3\omega})} \cdot I_{dc} \cdot cos(3\omega t) \ , \qquad (7.16)$$

where $k_{3\omega|(I_{osc}*v_{o,3\omega})}$ and $k_{3\omega|(I_{dc}*v_{inj,3\omega})}$ are conversion coefficients.

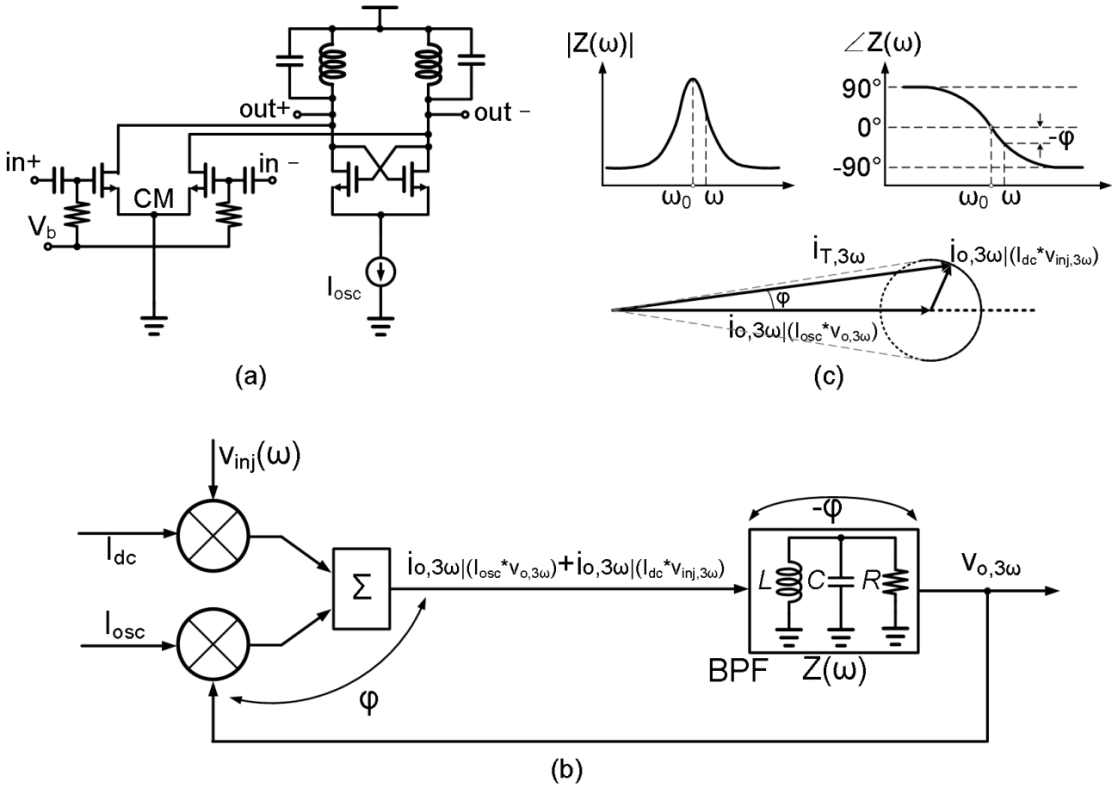

Fig. 7.8 Conventional ILFT: (a) schematic, (b) behavioral model, (c) phasor diagram

Proper operation of the injection-locked frequency tripler requires that the total phase shift around the loop is 0 and that the open-loop gain should be larger than unity, which is easily satisfied as long as it can self-oscillate. The phase condition is analyzed

by the phasor diagram in Fig. 7.8 (c). The phase contributed by the LC tank at frequency ω should be compensated by the phase angle φ between the current component $i_{o,3\omega|(I_{osc}*v_{o,3\omega})}$ and the total summed current $i_{T,3\omega}$. Similar to the analysis in [18], the angular frequency locking range ω_L can be derived as:

$$\omega_L = \frac{\omega_o}{2Q} \cdot \eta \cdot \frac{1}{\sqrt{1-\eta^2}} , \tag{7.17}$$

$$\eta = \frac{k_{3\omega|\left(I_{dc}*v_{inj,3\omega}\right)} \cdot I_{dc}}{k_{3\omega|(I_{osc}*v_{o,3\omega})} \cdot I_{osc}} , \tag{7.18}$$

where Q is the quality factor of the LC tank and η is defined as the injection ratio. In general, $i_{o,3\omega|(I_{osc}*v_{o,3\omega})}$ is designed to be the minimum value to sustain self-oscillation. Therefore, besides tuning the resonant frequency ω_o, the locking range can be improved by increasing $i_{o,3\omega|(I_{dc}*v_{inj,3\omega})}$. Larger I_{dc} would require larger injection devices, which is typically not desired, not only because of more loading to the previous stage, but also because of larger power consumed due to more DC current drawn by the injection branch and more self-oscillation current needed to compensate the quality factor degradation of LC tank. The conversion coefficient $k_{o,3\omega|(I_{dc}*v_{inj,3\omega})}$ could be boosted by operating the input transistors in sub-threshold region, but it's still quite small. As a result, the locking range of frequency tripler appears very narrow.

As long as the nonlinearity of transistors is not an efficient way to convert the input fundamental tone to third-order harmonic, another frequency conversion mechanism, mixing, is proposed to boost the conversion efficiency. Instead of directly routed to ground, the common-mode node CM is connected to ground through an inductor L_t, which resonates with the parasitic capacitance at 2ω, as shown in Fig. 7.9 (a). As such, a second-harmonic tone $v_{cm,2\omega}$ exists in Node CM, and thus it's mixed with the input

fundament tone to generate a third-order harmonic tone $i_{o,3\omega|(v_{inj,\omega}*v_{CM,2\omega})}$. At the same time, the previous tone $i_{o,3\omega|(I_{dc}*v_{inj,3\omega})}$ remains the same, since the common-mode node is virtually ground for odd-order harmonics. The corresponding behavioral model and phasor diagram are shown in Fig. 7.9 (b) and (c), respectively. The maximum achievable angle φ' becomes significantly larger that locking range enhancement is achieved:

$$\omega_L{}' = \frac{\omega_o}{2Q} \cdot \eta' \cdot \frac{1}{\sqrt{1-\eta'^2}} , \tag{7.19}$$

$$\eta' = \frac{k_{3\omega|(I_{dc}*v_{inj,3\omega})} \cdot I_{dc} + i_{o,3\omega|(v_{inj,\omega}*v_{CM,2\omega})}}{k_{3\omega|(I_{osc}*v_{o,3\omega})} \cdot I_{osc}} , \tag{7.20}$$

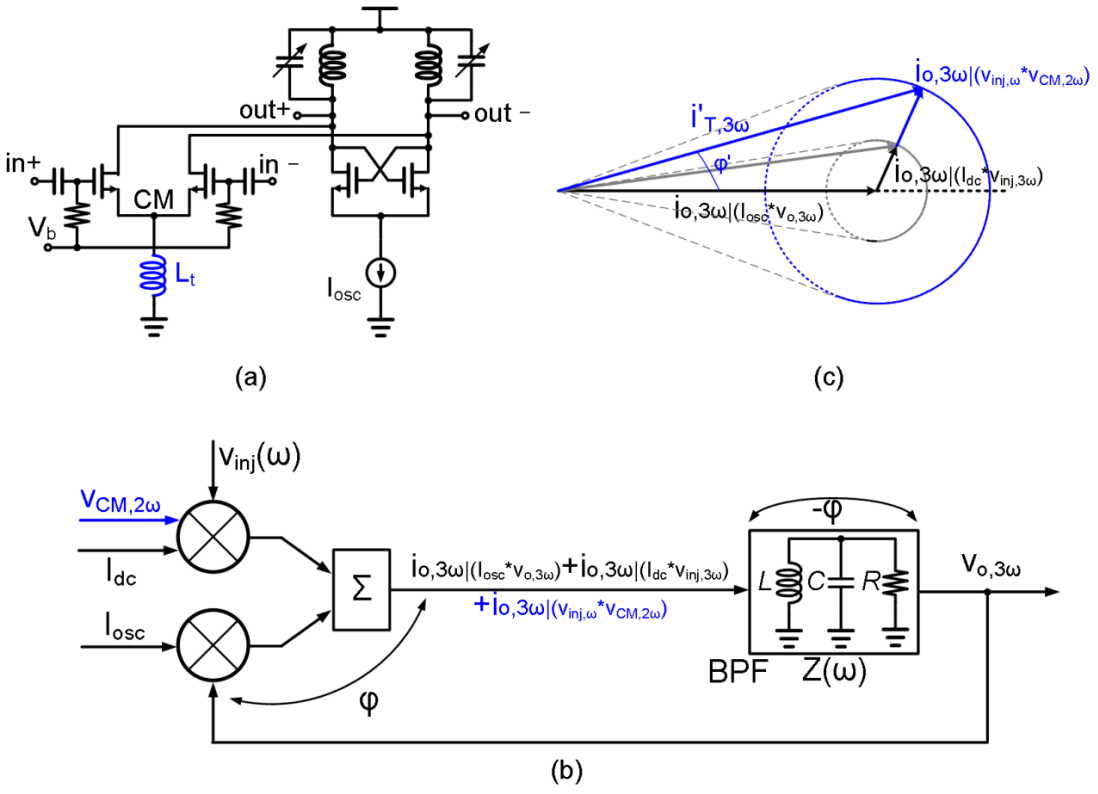

Fig. 7.9 Proposed ILFT: (a) schematic, (b) behavioral model, (c) phasor diagram

Simulations in SprectreRF have been performed to verify the efficiency improvement of frequency conversion. As shown in Fig. 7.10, the single-ended third-

order tone of the injection current gets significantly boosted from 3.6μA to 139μA, and thus locking range enhancement is expected. At the same time, the second-harmonic tone gets degraded from 322μA to 116μA, due to the transconductance degeneration at 2ω by the impedance of the inductor L_t. Furthermore, the simulation result of the frequency tripler shows that the locking range can be improved from < 200MHz to be around 2GHz. Apparently, proposed injection-locked frequency tripler improves the locking range and help to suppress the second-harmonic tone at the output with neither adding extra loading to the previous stage nor consuming extra power.

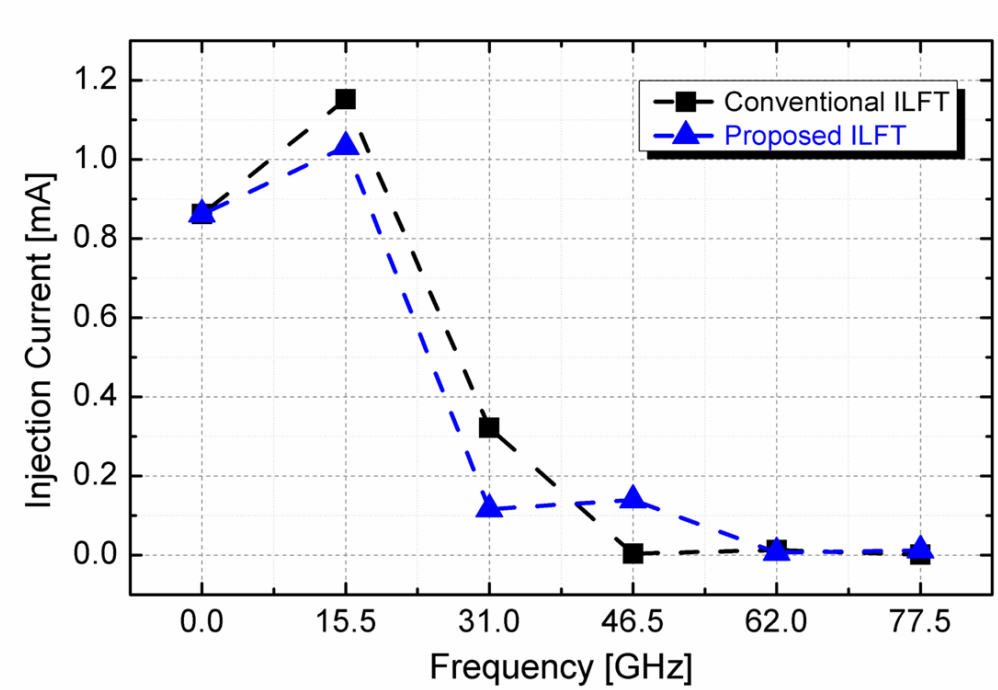

Fig. 7.10 Injection Current of (a) Conventional ILFT, (b) Proposed ILFT

7.4.3 Virtual Third-Order Standing-Wave Mode Buffer

Each of the 4-path outputs has to drive all of the four MUXs and thus the loading is severely large that conventional buffer based on simple LC tank could not provide

enough voltage swing. The buffer proposed in [22] can make the effective loading appear smaller by transforming the impedance along the synthesized transmission line using inductors and capacitors, as shown in Fig. 7.11 (a). However, the inductance ratio L_1/L_2 and capacitance ratio C_1/C_2 are restricted to be 1/2 and 1, respectively. The parameter optimization of both the inductance and capacitance is not quite flexible that it's not suitable for this application, considering the capacitance C_1 at the near end of the input gm cell are much smaller than C_2 which is at the far end.

To derive a more general result, the behavioral model in Fig. 7.11 (a) is restudied here. The voltage amplitude of the standing-wave along the synthesized transmission line is shown in Fig. 7.11 (b). There are two peaks at 1/4 λ and 3/4 λ and two voltage notches at 0 and 1/2 λ. A virtual ground exists somewhere inside L_2 and dividing L_2 into two parts: xL_2 and $(1\text{-}x)L_2$. The two lumped LC networks looking left and right from the virtual ground point have the same resonant frequency [22]:

$$\omega = \frac{1}{\sqrt{(L_1 || xL_2)\, C_1}} = \frac{1}{\sqrt{(1-x)\, L_2 C_2}} \ , \tag{7.21}$$

It's desired to have voltages peaks at point A and the output. From the perspectives of wave propagation, the equivalent lengths of the transmission line are 1/4 λ and 1/2 λ by looking left and right from point A. Therefore, it's approximately true that:

$$\frac{1}{\sqrt{L_1 C_1}} = 2 \cdot \frac{1}{\sqrt{L_2 C_2}} \ \rightarrow \ L_1 = \frac{L_2}{4} \cdot \frac{C_2}{C_1} = \frac{n}{4} \cdot L_2 \ , \tag{7.22}$$

where n is defined as the capacitance ratio. Combining Eq. (7.21) with (7.22), it can be derived that:

$$x^2 + \frac{n-3}{4} x - \frac{n}{4} = 0 \ , \tag{7.23}$$

$$0 \leq x \leq 1 \quad \rightarrow \quad n \geq 3 \ . \tag{7.24}$$

For the case in this work, n is around 4 and thus x is derived to be 0.88, hence the peak frequency can be expressed as:

$$\omega = \frac{1.46}{\sqrt{L_1 C_1}} = \frac{2.92}{\sqrt{L_2 C_2}} \ . \tag{7.25}$$

Comparing with directly driving the loading capacitance C_2, the frequency is boosted to be twice higher. Along the LC network, a virtual third-order standing-wave mode

Based on these analyses, a buffer is proposed, as shown in Fig. 7.11 (c). L_1 and L_2 are implemented with spiral inductor and transmission line, respectively. Along the LC network, there is a virtual third-order standing-wave. The transmission line is differential and thus a virtual ground exists that no dedicated metal ground plane above the substrate is used to ease the layout, as shown in Fig. 7.11 (d).

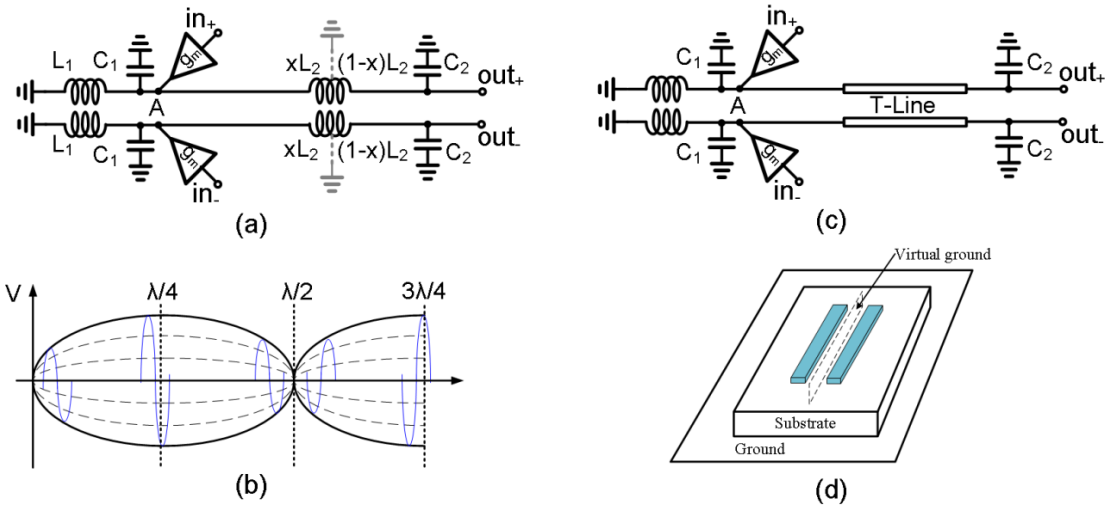

Fig. 7.11 Proposed standing-wave mode buffer: (a) Behavioral model, (b) Standing wave, (c) Implementation, (d) Transmission line

7.4.4 Phase Detector with Low-Pass Filter

The phase detector is implemented by a mixer, in which two Gilbert cells are combined with cross-connected inputs [20], resulting in a highly symmetrical input loading, as shown in Fig. 7.12. The output is composed of RC network featuring low-pass filtering.

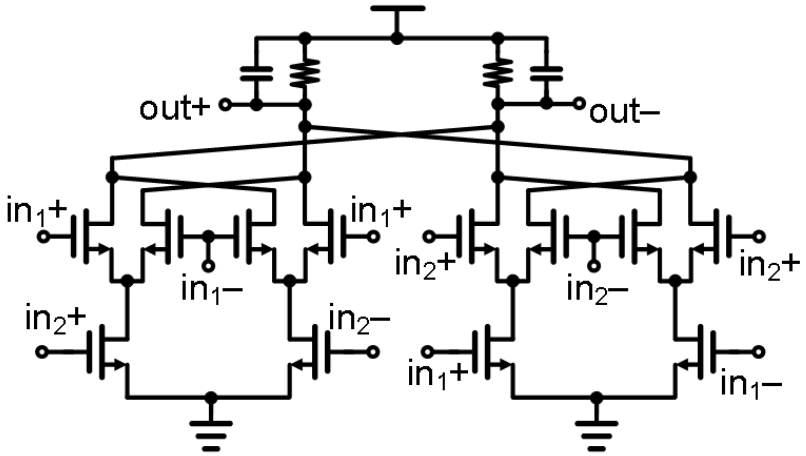

Fig. 7.12 Highly symmetric phase detector with RC low-pass filter

7.5 Experimental Results

The whole LO generation in Fig. 7.3 is fabricated in a Low-Power 65nm CMOS process with 1 poly and 6 metal layers. Fig. 7.13 shows the chip micrograph, which occupies a core area of 2.0 × 1.4 mm^2. Highly symmetrical layout is implemented by placing the four LO generation chain in the four corners, while the phase detection is located at the center. The phase shifts from the buffer outputs to MUX inputs are designed to be ideally symmetrical among the 4 paths. As such, the phase offset introduced by the mux and routing wires of each path is the same and thus the phase differences of the MUX inputs is equal to that of the buffer output. Any residual phase

errors due to mismatches can be further detected and fine-tuned by the baseband in a phased-array system depending on the requirement of applications.

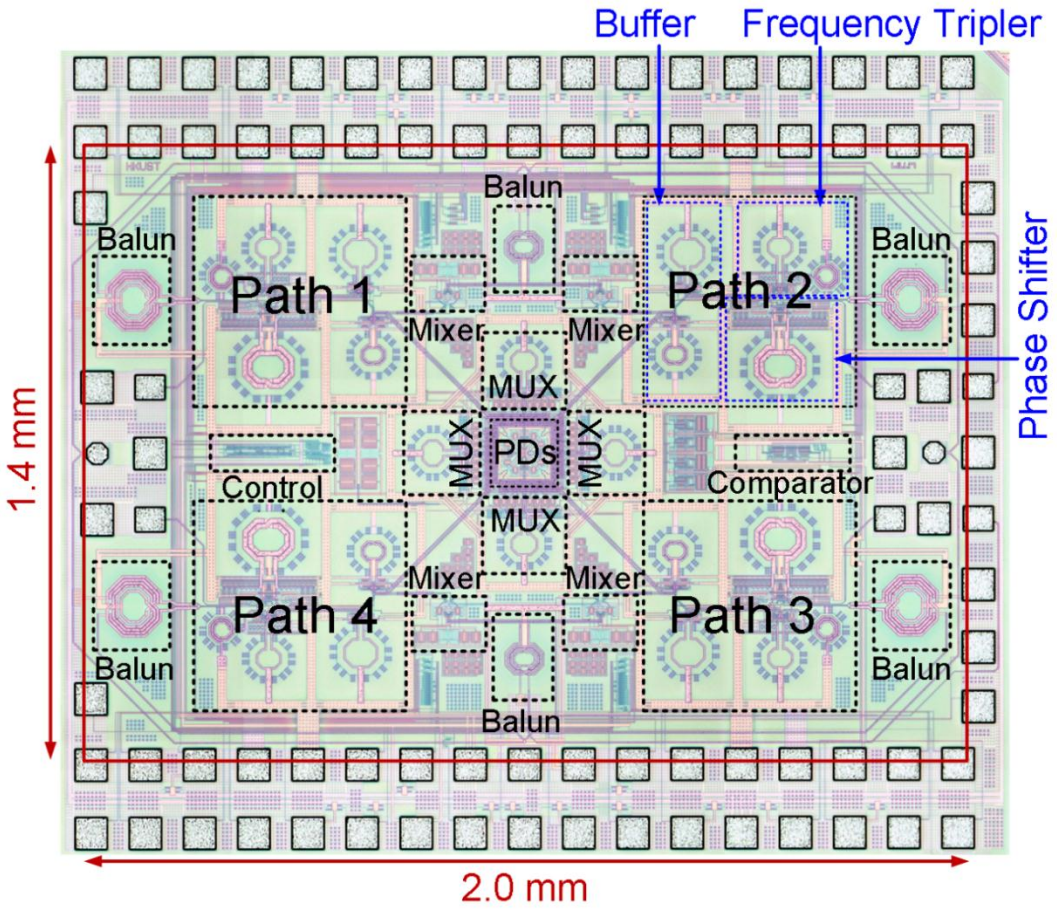

Fig. 7.13 Chip micrograph

7.5.1 Measured Phase Shift

Fig. 7.14 shows the measured phase tuning curves, which verify that the phase shift range is larger than –90° ~ 90° for all the 4 channels of IEEE 802.15.3c standard. The non-monotonicity is merely due to the overlapping of the two SCA groups, which should not be a problem by properly selecting the digital words in FSM. The amplitude variation is shown in Fig. 7.15. It's as small as within ±0.35dB thanks to the injection locking mechanism utilized in both the phase shifters and frequency triplers.

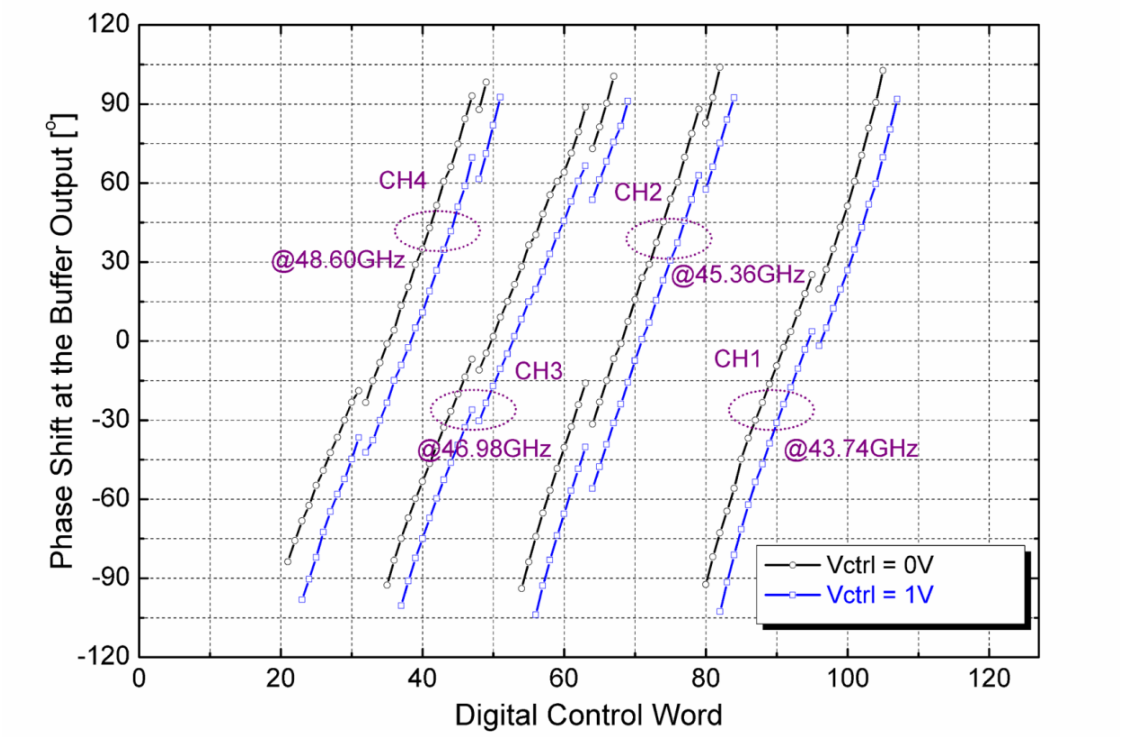

Fig. 7.14 Phase tuning curves

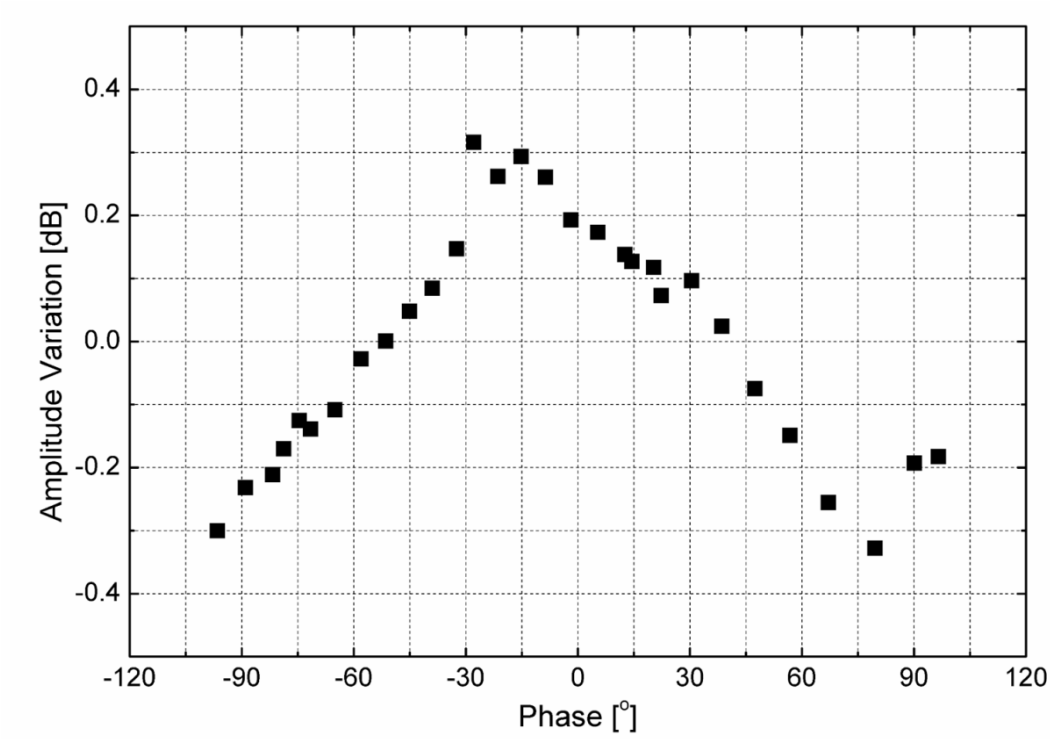

Fig. 7.15 Amplitude variations

7.5.2 Measured Phase Noise

To further verify the correct operation of the linear-phase-shift generation, the phase noise of input and output signals of the LO generator is measured. As shown in Fig. 7.16, the output phase noise closely follows the input phase noise. Compared with input, the output phase noise is degraded around 9.5 dB, which is theoretically expected because the output frequency is three times as the input frequency.

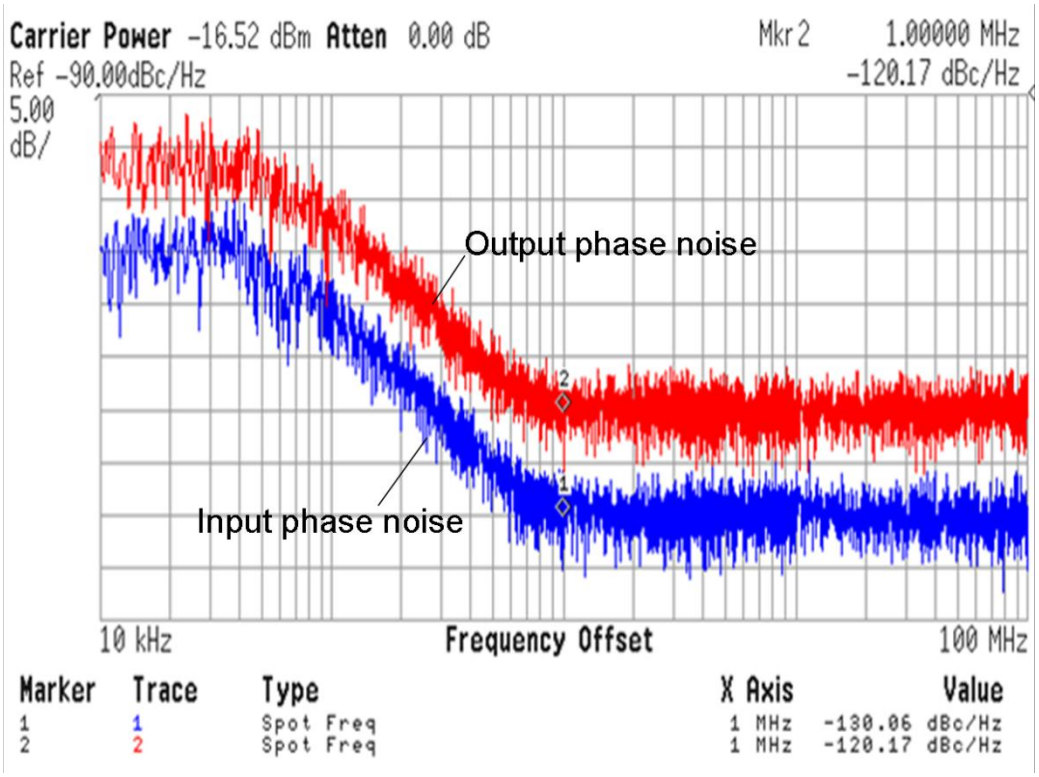

Fig. 7.16 Measured input and output phase noise of linear-phase-shift chain

7.5.3 Measured Phase Tuning

Fig. 7.17 shows the transient waveforms. Using the proposed automatic tuning followed by exhaustively tuning for a 22.5° phase difference between adjacent paths, an RMS phase error of 0.93° of each path is measured, comparing with 13.12° before tuning. The maximum phase error is reduced from 21.93° to 1.32°.

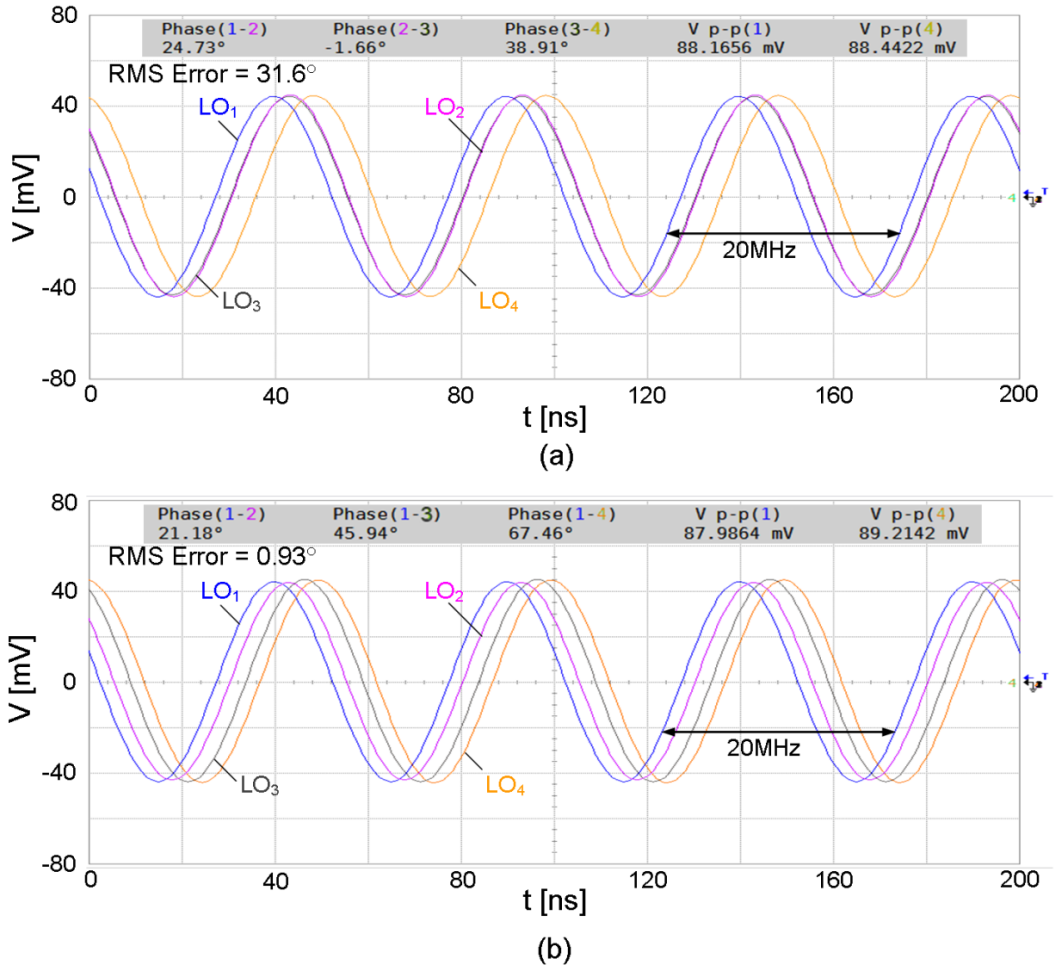

Fig. 7.17 Measured transient waveforms: (a) before tuning, (b) after tuning

7.5.4 Mismatch Characterization

To characterize the mismatch among four different paths, the phase shifters located farthest from each other are enabled to be self-oscillating one at a time while the LO input centered at 15GHz from an off-chip signal source is disabled. The digital signal $D_{ctrl1\text{-}4}$ for coarse tuning is set to minimum or maximum value while the analog signal $V_{ctrl1\text{-}4}$ for fine tuning is varied from 0 to 1V. The frequency tuning curves of the phase shifters in the 4 paths are shown in Fig. 7.18. Statistically, the minimum, average and maximum absolute frequency mismatches are 0.007%, 0.074% and 0.181%, respectively.

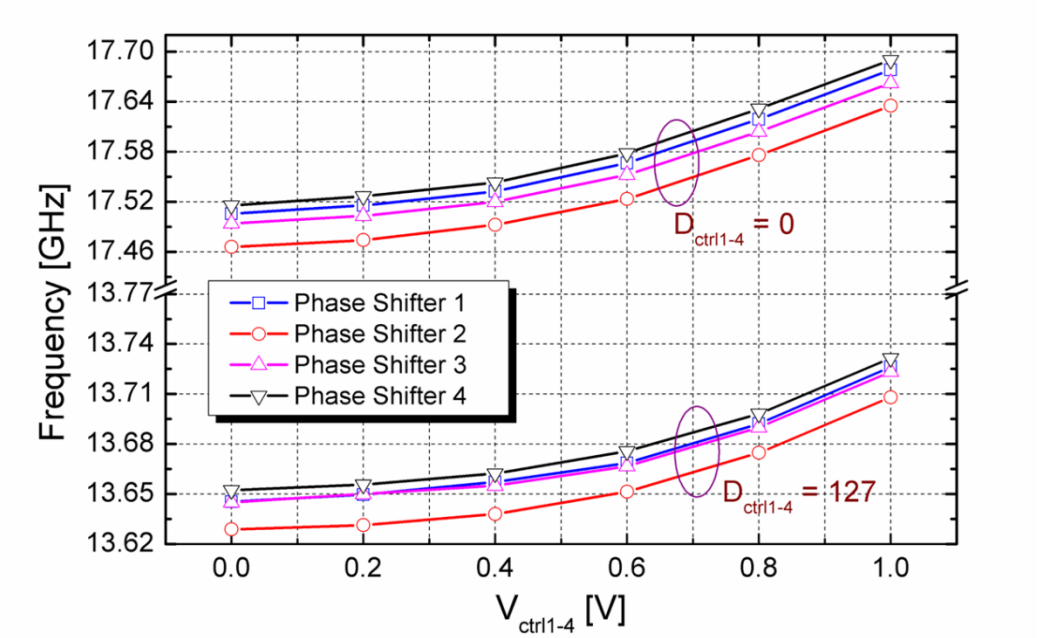

Fig. 7.18 Measured frequency tuning curves of phase shifters to characterize mismatches

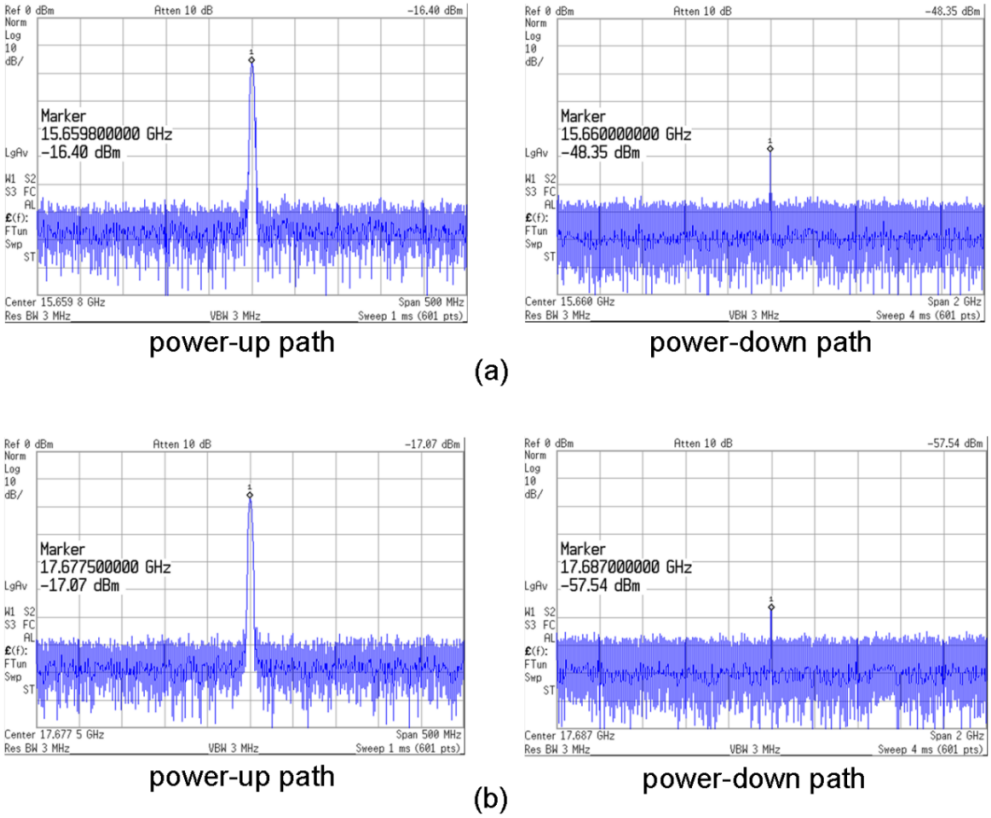

Fig. 7.19 Measured spectrum of power-up path and its neighboring power-down path at (a) 15.66GHz and (b) 17.68GHz

7.5.5 Isolation Characterization

To characterize the isolation between different paths, a phase shifter is turned on and the spectrum is measured at both its open-drain buffer output and the nearest neighboring path output. As shown in Fig. 7.19, the isolations are better than 32dB at two frequencies.

7.5.6 Performance Summary

Table 7.1 summarizes and compares the performance with recently published state-of-art LO generation for phased-arrays. LO phase shift generation system proposed this work covers a frequency range from 42.75 to 49.5GHz, with amplitude mismatch within ±0.35dB, phase resolution of 22.5°, RMS phase error of 0.93°. With 1.0-V supply, the LO generation core consumes a current of 55mA while the automatic phase detection and tuning part draws a current of 30mA.

7.6 Conclusion

An LO generation system for phased-array receivers according to the IEEE 802.15.3c standard with automatic phase tuning has been developed and successfully demonstrated in a standard 65nm CMOS technology. The design and circuit implementation of the key building blocks including phase shifter, injection-locked frequency tripler, virtual third-order standing-wave mode buffer, and phase detector were discussed. With the proposed variable linear-phase-shift chain and successive-approximation algorithm, linear phase shift with automatic tuning has been achieved and is able to cover all of the four channels with phase shift range larger than –90° ~

90°, very small RMS phase error and amplitude variations.

Table 7. 1 Measured performance summary and comparison with other LO generation system for phased-arrays.

Ref.	This work	[11] [Natarajan '06]	[19] [Scheir, '08]	[22] [Hashemi, '05]	[23] [Chan, '10]
Frequency [GHz]	42.75 ~ 49.5	50.3 ~ 55.5	43.7 ~ 51.7	18.8 ~ 21.0	57.0
Amplitude Mismatch [dB]	±0.35	1.5	-4.0 ~ 1.6	N/A	N/A
Phase Resolution [°]	22.5	N/A	45.0	22.5	N/A
Phase Error [°]	0.93	0.5 *	5.7	N/A	N/A
Path No.	4	4	2	8	4
Supply [V]	1.0	2.5	1.2	2.5	1.0
Current [mA]	55 (core) 30 (auto. tuning)	56	28.7	76.4 **	310
Technology	65nm CMOS	120nm SiGe BiCMOS	90nm CMOS	180nm SiGe HBT CMOS	65nm CMOS

* For 5-bit DAC

** Including a phased-locked loop.

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Chapter 8

4-Path Phased-Array Receiver with Closed-Loop Beamforming

8.1 Introduction

To relax the link budget due to large path loss and improve the spectral efficiency for high-data-rate wireless communication at mm-Wave frequencies, phased-arrays which feature spatial power combining and electrical beamforming capabilities are widely used. In this chapter, the whole 4-path phased-array receiver RF front-end is presented.

8.2 Block diagram

The block diagram of the proposed 4-element phased-array receiver system is shown in Fig. 8.1. Each element of the RFE employs a dual-conversion zero-IF architecture with the first and second LO signals centered at 45GHz and 15GHz respectively. By implementing the variable phase shifters in the first LO paths, the linearity, noise figure and bandwidth requirements are significantly relaxed. To compensate for the signal gain mismatch due to PVT variations among the 4 elements, variable g_m stages are included in each path. The second down-conversion stages are shared by two neighboring elements thus only two IF I/Q paths are required. As such, the array pattern can be reconfigured to produce either two independent beams

concurrently, each by two-element groups, or one single beam by all four elements, depending on the application. The phase shift generation scheme discussed in Chapter 7, consisting of an injection-locked oscillator based phase shifter followed by an injection-locked frequency tripler, is utilized in the first LO path to generate a linear phase shift from -90 ° to 90 ° with LO amplitude variations within ±0.4dB. The control signals D_{phn} and V_{phn} are for digital coarse tuning and analog fine tuning, respectively. For the second LO, the same external signal is converted to quadrature by a balun and poly-phase filter to injection-lock the QVCO, which helps to correct both the phase and amplitude errors of the quadrature signals. LC loaded buffers are then employed to increase their driving capabilities and to allow fine I/Q phase error calibration through independently controlled varactors.

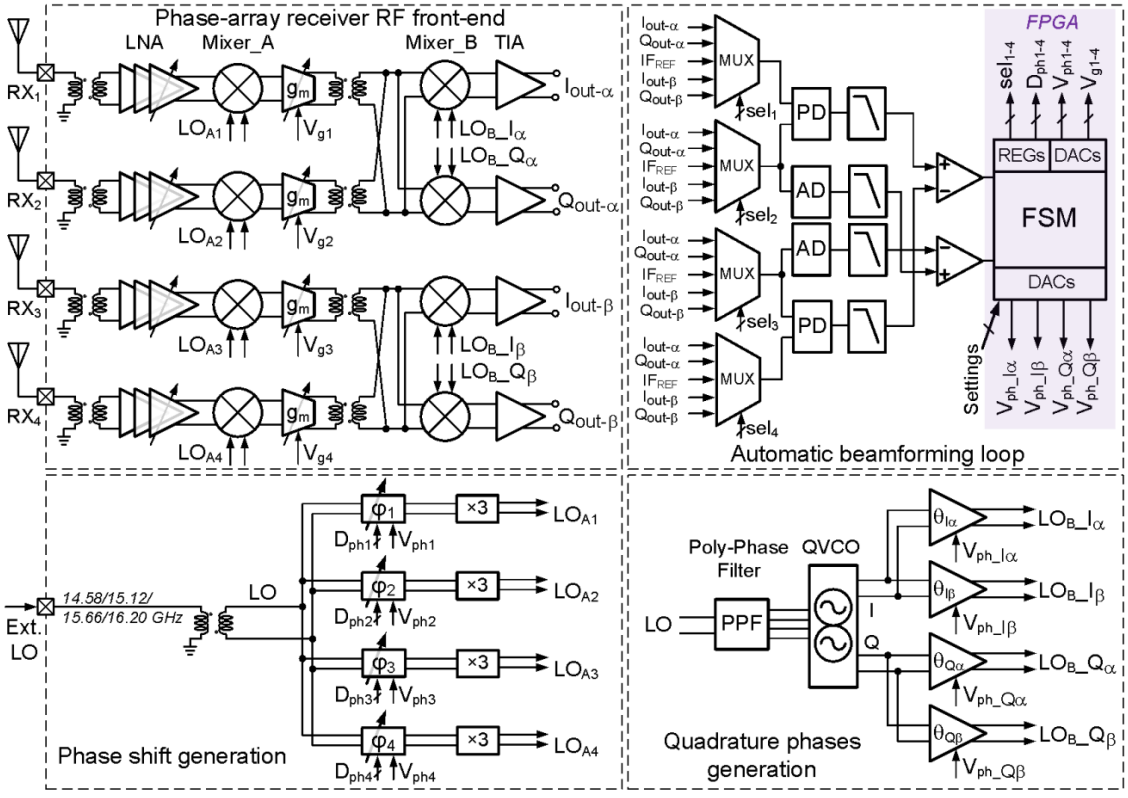

Fig. 8.1 Block diagram of proposed 4-path phased-array receiver system

To achieve best peak-to-null ratio of the phased-array receiver, the variable phase shift and gain of each element needs to be set properly. Conventionally, these optimal settings are determined through exhaustive searching algorithms and stored in a look-up-table (LUT) to be selected by the baseband every time the beam angle changes. Due to process variations, the LUT varies from chip to chip and is thus very expensive to obtain as the LUT setup time grows exponentially with the number of elements. A phase detection and tuning loop at the LO paths to automatically achieve the desired phase shifts without the need for exhaustive searching helps to significantly reduce this setup time [1]. This high frequency loop, however, requires not only a highly symmetrical layout, but also large chip area due to the large number of inductors needed. To resolve this, the phased array detects the phase error using the lower frequency IF outputs and IF_{REF}, instead of the LO signals, to drive the phase detectors (PDs). Amplitude detectors (ADs) are also implemented to equalize the gain of each element. The control generation is implemented using an FPGA to automatically steer the beam directions as shown in Fig. 8.1.

8.3 Closed-Loop Beamforming

To detect and compare the gain and phase contributed by each element, each RFE should have RF input with equal amplitude and phase. This can be easily implemented by wireless transmitting a signal at a point which measures the same distance to the antenna of each element. Without antennas implemented in this work, an external signal is symmetrically routed to all 4 elements and injected to their respective LNA inputs. The proposed closed-loop beamforming is obtained by sequentially performing signal path gain equalization and LO phase shift tuning. Gain equalization is done by selecting

each of the 4 IF output and comparing it with IF_{REF} to tune the variable g_m stages. Phase shift tuning is mainly based on successive approaching algorithm in [1] which can tune any phase of $90°/2^k$ by successively obtaining $90°/2^i$, with i starting from 0, 1, …, k.

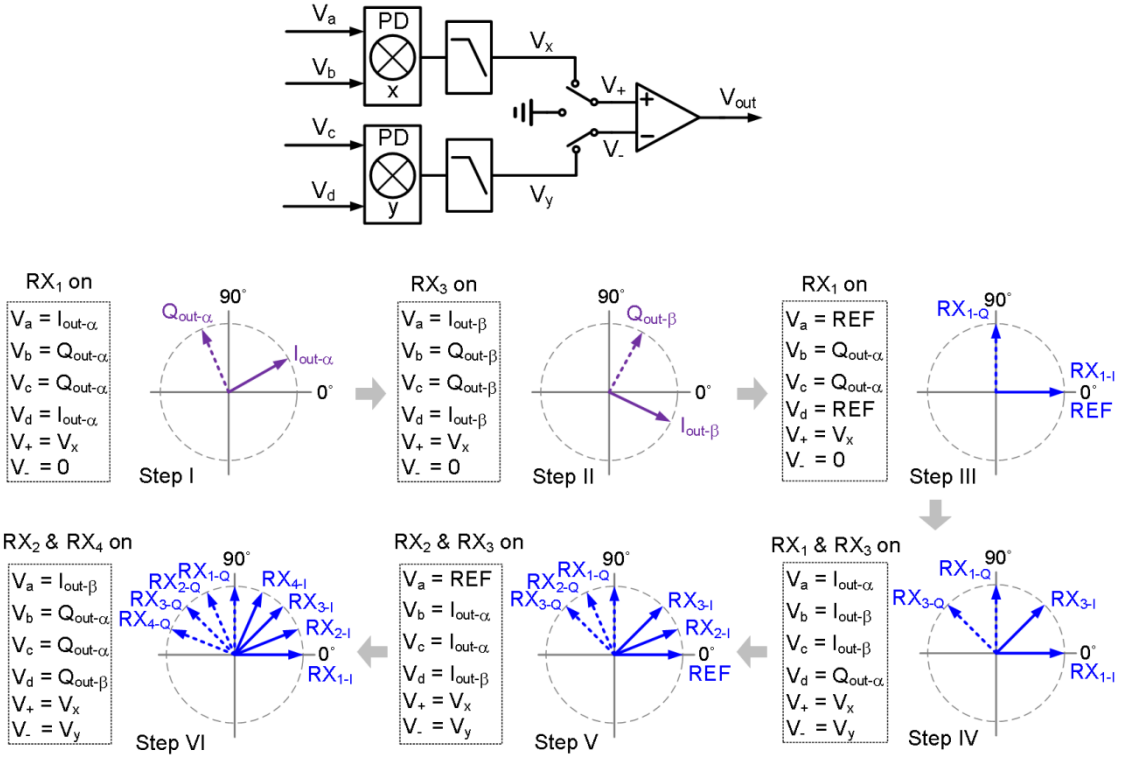

Fig. 8.2 Proposed closed-loop beamforming mainly based on successive approaching algorithm

An example of automatic beamforming with Δ22.5° phase between neighboring elements is illustrated in Fig. 8.2. After gain equalization, the amplitude of each IF output is the same as IF_{REF}. In Step I and II, RX_1 and RX_2 are separately turned on and traditional IQ calibration is performed by tuning the buffers of the second LO thus eliminating I/Q errors. In Step III, only RX_1 is enabled and $\angle LO_{A1}$ is tuned such that $\angle RX_{1\text{-}I} = \angle IF_{REF} = 0°$ and $\angle RX_{1\text{-}Q} = 90°$. In Step IV, both RX_1 and RX_3 are enabled. By using $\angle RX_{1\text{-}I}$ and $\angle RX_{1\text{-}Q}$ as reference and tuning $\angle LO_{A3}$ until $V_+ = V_-$, $\angle RX_{3\text{-}I}$ is set

to 45°. After two more similar steps, $\angle RX_{1\text{-}I}$, $\angle RX_{2\text{-}I}$, $\angle RX_{3\text{-}I}$ and $\angle RX_{4\text{-}I}$ can be tuned to be 0°, 22.5°, 45°, and 67.5°, respectively. Since the phase contributed by each signal path has been taken into account, the phase mismatch at signal path is intrinsically compensated. As the phase tuning is done at the LO path, there is minimal influence on the amplitude in the RF signal path, thus no convergence problems exist with the dual-loop control.

8.4 Proposed RF Front-End with Hybrid-Mode Mixing

8.4.1 Circuit Design and Implementation

The RFE block diagram of a single element is shown in Fig. 8.3 along with detailed schematics of the critical blocks. The proposed hybrid-mode architecture improves the RFE's linearity which is critical for 60GHz phased-array receiver [2], with only degrading the gain and noise figure little. This is done by operating the LNA and Mixer_A in voltage mode for large gain and low NF and then switching to current mode in Mixer_B where linearity is dominant to avoid the typically large signal swings.

A 1:1 balun is used to convert the single-ended signal from the antenna to differential for the LNA while also acting as an input matching network. The LNA is composed of three stages. A common source structure is used for the first two stages for low NF and is stabilized by neutralization capacitors. Their peak frequencies are staggered such that the 3dB bandwidth covers a range from 57 to 66 GHz. Variable gain is implemented by current-steering in the third stage to allow the NF to be traded-off with linearity depending on the input power level. The LNA output current is directly transformer-coupled into the switching pairs of Mixer_A to improve linearity by

eliminating the V-to-I stage traditionally present in the tail of the mixer. The down-converted signal in current domain gets boosted with the LC load of the mixer and its following g_m stage. Adjacent 2-path IF signals are then combined in current domain using a transformer which also provides current gain. The cumulative gain is sufficient for the system and suppresses the noise contribution from subsequent stages. The transformers discussed above simplify the floor-plan by acting as interconnections and resonate out the parasitic capacitances. Mixer_B is designed as a current-mode passive mixer to further improve linearity, reduce power consumption and lower 1/f noise. A trans-impedance amplifier then performs the final I-to-V conversion for the baseband.

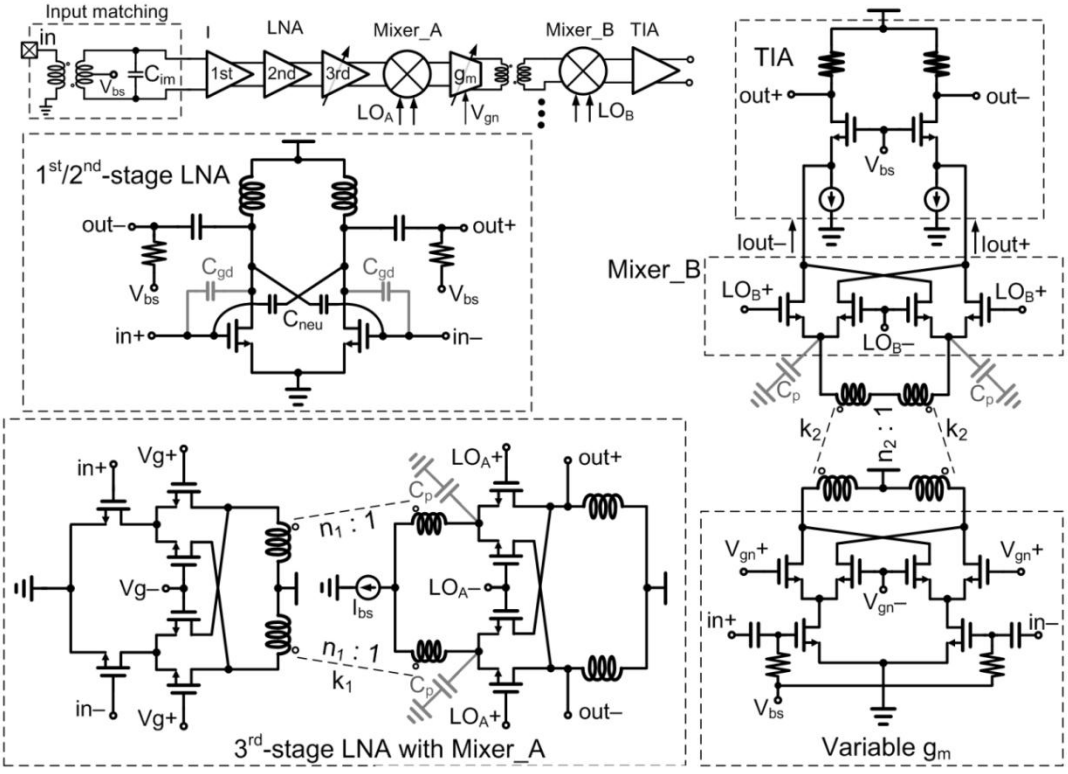

Fig. 8.3 Schematic of proposed hybrid-mode RF front-end, including 3-stage LNA, Mixer_A, variable gm, Mixer_B and TIA

8.4.2 Analysis of Proposed Hybrid-Mode Architecture

The schematics of the building blocks from the loading of the 3rd-stage LNA to baseband output are shown in Fig. 8.4.

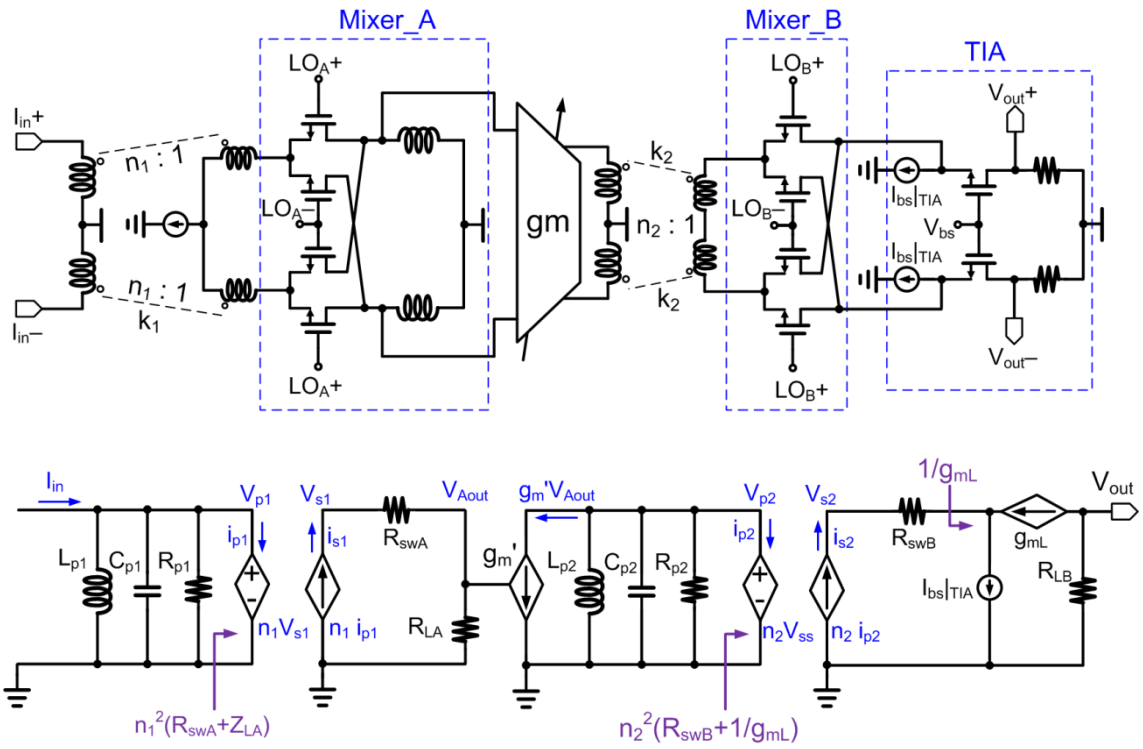

Fig. 8.4 Analysis of proposed RF front-end with transformer based hybrid-mode mixing

In the equivalent model, the coupling factors k_1 and k_2 are assumed to 1 for simplicity. And hence the equation of the relationship between V_{out} and I_{in} can be derived as:

$$\frac{V_{out}}{I_{in}} = g_m{}' \cdot \alpha_A \cdot \alpha_B \cdot n_1 \cdot n_2 \frac{R_{p1} \cdot R_{p2} \cdot R_{LA} \cdot R_{LB}}{\left[R_{p1} + n_1^2\left(R_{swA} + R_{LA}\right)\right]\left[R_{p2} + n_2^2\left(R_{swB} + 1/g_{mL}\right)\right]}, \quad (8.1)$$

where α_A and α_B are the switching efficiencies of Mixer_A and Mixer_B respectively.

To achieve the highest gain, the turn ratios n_1 and n_2 should be the optimal values which are express as:

$$n_1 = \sqrt{R_{p1} \big/ \left(R_{swA} \cdot R_{LA} \right)} \ , \tag{8.2}$$

and

$$n_2 = \sqrt{R_{p2} \big/ \left(R_{swB} + 1/g_{mL} \right)} \ , \tag{8.3}$$

respectively.

In general, the linearity is limited because of the non-linearity of V-to-I g_m devices. By directly transformer-coupling the output current of the 3rd- stage LNA into the switching pairs of Mixer_A, the V-to-I stage traditionally presenting in the tail of the mixer is eliminated. Therefore, the voltage swings $V_{p1\pm}$ and $V_{p2\pm}$ become the main concern. Due to the impedance transformation by the transformer, the equivalent resistive load of the secondary coil degrades the quality factor of the primary coil and thus $V_{p1\pm}$ and $V_{p2\pm}$ get reduced that they are not the bottle neck of system linearity. Output voltage $V_{outA\pm}$ of Mixer_A is typically out of consideration, as long as the down-converted current at 15GHz is only a small portion of input current at 60GHz due to the low switching efficiency of CMOS FETs. Therefore, the linearity of the whole RF front-end is determined by the TIA, whose bias current $I_{bs|TIA}$ is designed to be 2~3 times larger the maximum AC current input to the current buffer. The AC current is derived to be:

$$I_x = I_{in} \cdot g_m{}' \cdot \alpha_A \cdot \alpha_B \cdot n_1 \cdot n_2 \frac{R_{p1} \cdot R_{p2} \cdot R_{LA}}{\left[R_{p1} + n_1^2 \left(R_{swA} + R_{LA} \right) \right] \left[R_{p2} + n_2^2 \left(R_{swB} + 1/g_{mL} \right) \right]}, \tag{8.4}$$

8.4.3 Comparison with Existing Architectures

8.4.3.1 Analysis of Voltage-Mode Mixing

The behavioral model of dual-conversion architecture with voltage-mode mixing is shown in Fig. 8.5. The relationship between the output and input can be derived as:

$$\frac{V_{out}}{I_{in}} = g_m R_p \cdot \alpha_A \cdot g_{mA} R_{LA} \cdot \alpha_B \cdot g_{mB} \cdot R_{LB} \ , \tag{8.5}$$

where α_A and α_B are the switching efficiencies of Mixer_A and Mixer_B respectively.

Due to the use of LC loading which has large equivalent impedance at resonant frequency, the voltage gain is typically large. However, the large input voltage swing of gm would make the transistor works out of saturation region and thus cause linearity problem. Generally, the last stage dominates the linearity and its corresponding voltage swing is derived as:

$$V_x = I_{in} \cdot g_m R_p \cdot \alpha_A \cdot g_{mA} R_{LA} \cdot \alpha_B \cdot g_{mB} \cdot \left(R_{swB} + R_{LB} \right) \ , \tag{8.6}$$

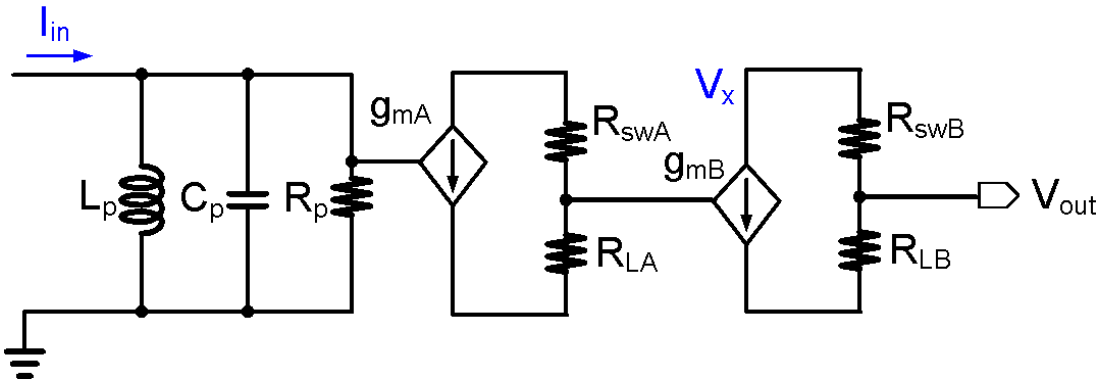

Fig. 8.5 Behavioral model of voltage-mode architecture

8.4.3.2 Analysis of Current-Mode Mixing

The behavioral model of dual-conversion architecture with current-mode mixing is shown in Fig. 8.6. The relationship between the output and input can be derived as:

$$V_{out} = I_{in} \cdot \alpha_A \cdot \alpha_B \cdot \frac{R_p}{R_p + R_{swA} + R_{swB} + 1/g_{mL}} \cdot R_{LB} \ , \tag{8.7}$$

where α_A and α_B are the switching efficiencies of Mixer_A and Mixer_B respectively.

Due to the cascading of two stages of mixers, the equivalent impedance of (R_{swA}+R_{swB}+1/g_{mL}) is not much smaller compared with R_p and thus only some of the input current will flow into the current buffer. As a result, even though the linearity of architecture with current-mode mixing is high, but the gain drops significantly. By properly sizing the bias current of the current buffer, the voltage swing V_x dominates the linearity and it is derived as:

$$V_x = I_{in} \cdot \frac{R_p \cdot \left(R_{swA} + R_{swB} + 1/g_{mL}\right)}{R_p + R_{swA} + R_{swB} + 1/g_{mL}} \ , \tag{8.8}$$

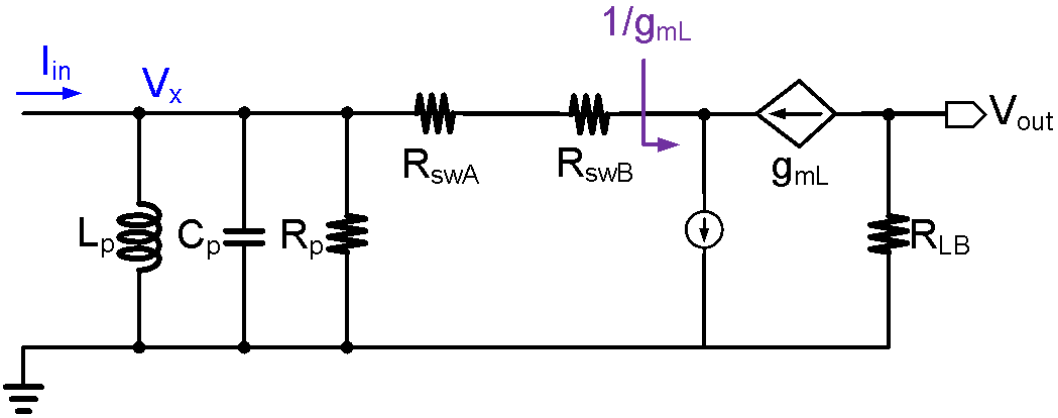

Fig. 8.6 Behavioral model of current-mode architecture

8.4.3.3 Comparison of voltage-mode, current-mode and hybrid-mode mixing

For dual-conversion architectures, conventional voltage-mode mixing features high gain but suffers from low linearity, while current-mode mixing features high linearity but suffers from low gain. In order to have sufficient gain for the system, current-mode mixing requires larger LNA gain than voltage-mode mixing, which is not cheap to achieve in terms of power, stability and linearity. Proposed hybrid-mode mixing achieves large gain thanks to the current gain of transformer and the voltage gain of the first stage voltage-mode mixing. At the same time, it achieves high linearity thanks to the lowing voltage swing by impedance transformation and highly linear current-mode passive mixing.

8.4.4 Layout Floor-plan and Consideration

Since signals up to 60-GHz are routed inside the phased-array receiver, the system performance will be largely layout dependent. Therefore, layout floor-plan should be designed carefully to minimize not only the effects from parasitic capacitance, inductance and resistance but also the mismatches among the 4 paths.

A highly symmetrical layout is achieved by placing those 4 receiver elements together with phase shift generation in four corners and locating the quadrature phase generation in the center. To further reduce the mismatches, dummy devices are inserted whenever necessary to guarantee local symmetry and global symmetry. Besides, the dc bias control signals are shielded with power lines. To minimize the magnetic coupling with each other through substrate, guard rings are used to shield the critical transformers, inductors and transistors.

Another critical issue for system integration is the long line interconnection between building blocks. In this work, transformers with input and output at two different sides are used to connect building blocks. As such, the parasitics are minimized. During design stage, some margins of parasitics are included for each building block.

8.5 Experimental Results

The whole phased-array receiver in Fig. 8.1 is fabricated in a 65nm CMOS process. The core area is 2.0×1.3 mm^2, as shown in Fig. 8.7.

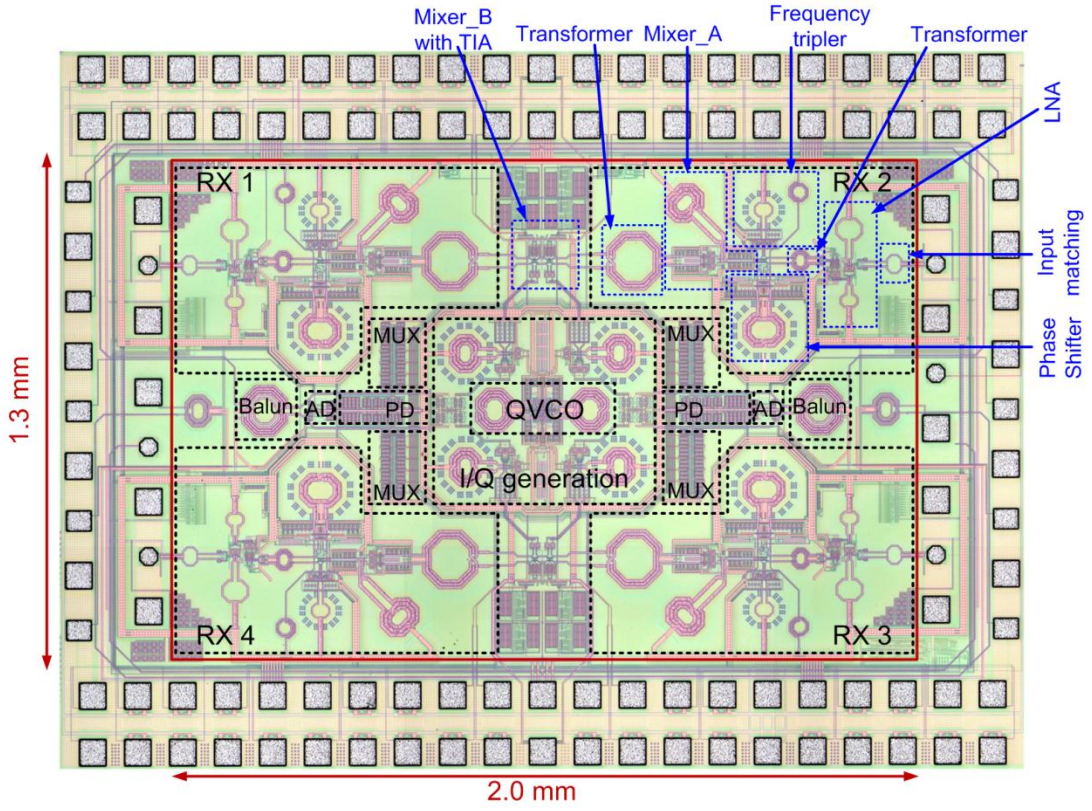

Fig. 8.7 Layout of proposed 4-path phased-array receiver

8.5.1 S_{11}

The S_{11} of the receiver is measured with a 67-GHz network analyzer, as shown in Fig. 8.8. The measured S_{11} is smaller than -10dB for the frequency from 54 to 67 GHz, which is sufficient to cover all frequency bands from 57 to 66 GHz, as show in Fig. 8.9.

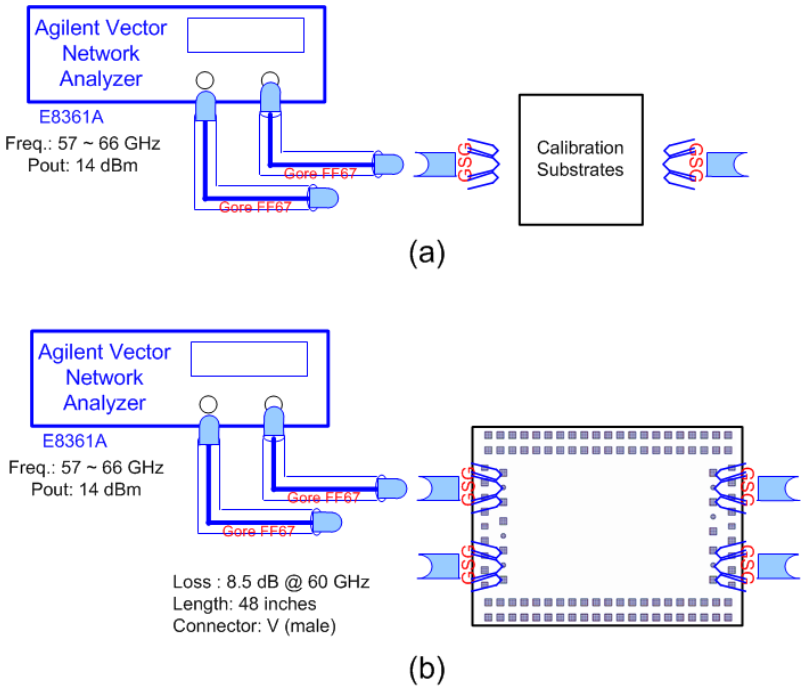

Fig. 8.8 Setup for S11 measurement: (a) calibration, (b) measurement

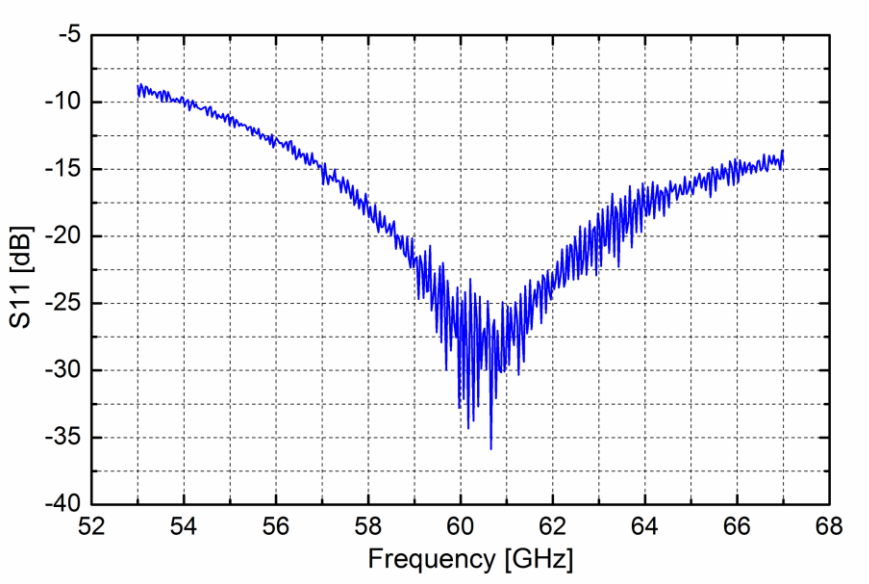

Fig. 8.9 Measured S_{11}

8.5.2 Conversion Gain

The gain is measured with the setup shown in Fig. 8.10.

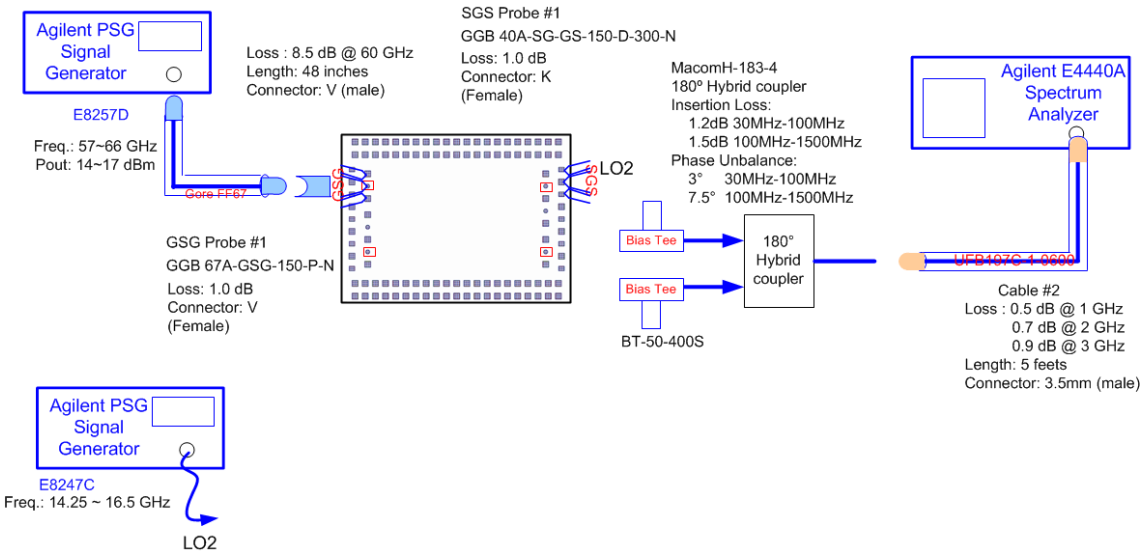

Fig. 8.10 Setup for conversion gain measurement

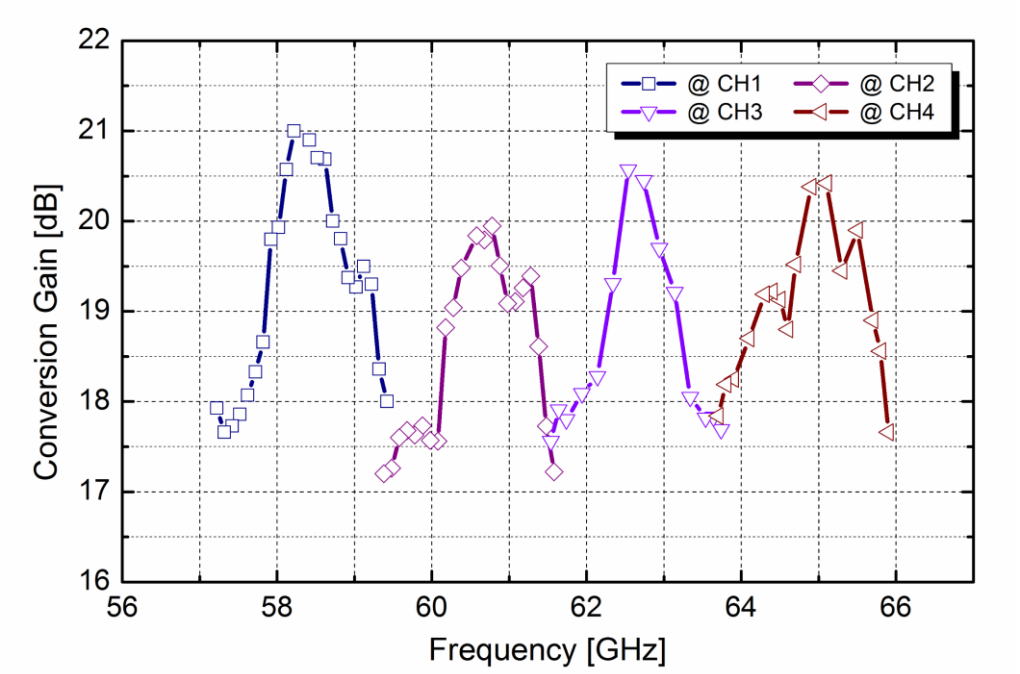

Fig. 8.11 Measured conversion gain

The conversion gain of the receiver at 4 channels specified in IEEE 802.15.3c is shown in Fig. 8.11. In high gain mode, the gain at the center frequency of each channel is larger than 20 dB and the -3dB bandwidth is larger than 2.16 GHz. The gain variation of each channel is due to the use of LC tank with switched-capacitor (SCA) as loading for Mixer_A and the variable gm stage. The band-pass filtering feature is useful to suppress interference signals at other channels. If it's not desired for some applications, LC load with shunt-peaking featuring wide bandwidth could help to reduce the gain variation.

8.5.3 Input Referred 1-dB Compression Point (IP_{1dB})

As shown in Fig. 8.12, the IP_{1dB} is around -12.5dBm in low gain mode.

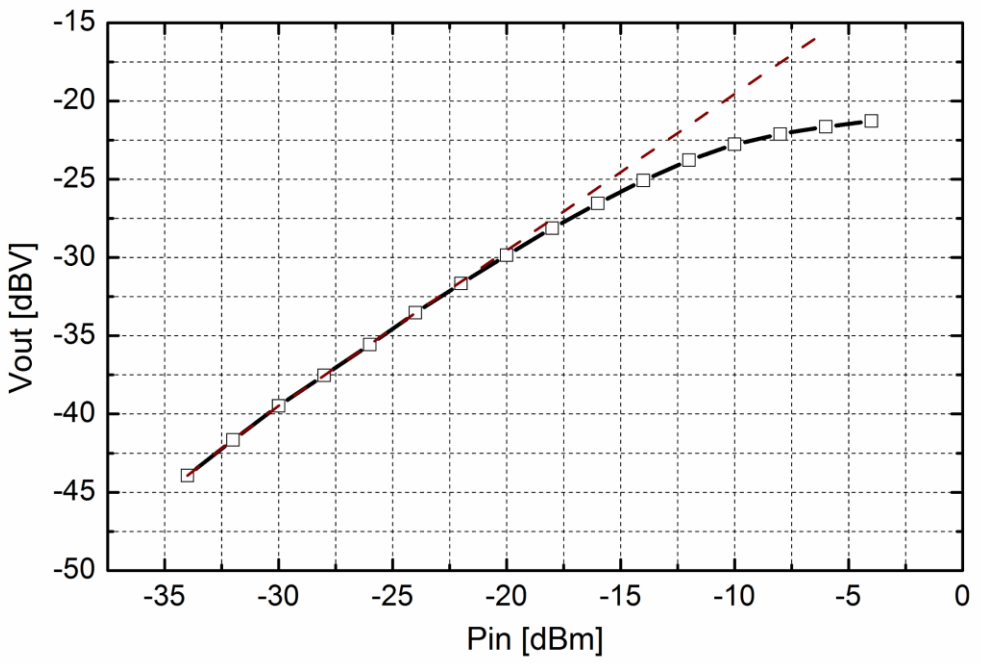

Fig. 8.12 Measured 1-dB compression point

8.5.4 Noise Figure

The noise figure in high-gain mode is measured with the setup shown in Fig. 8.13.

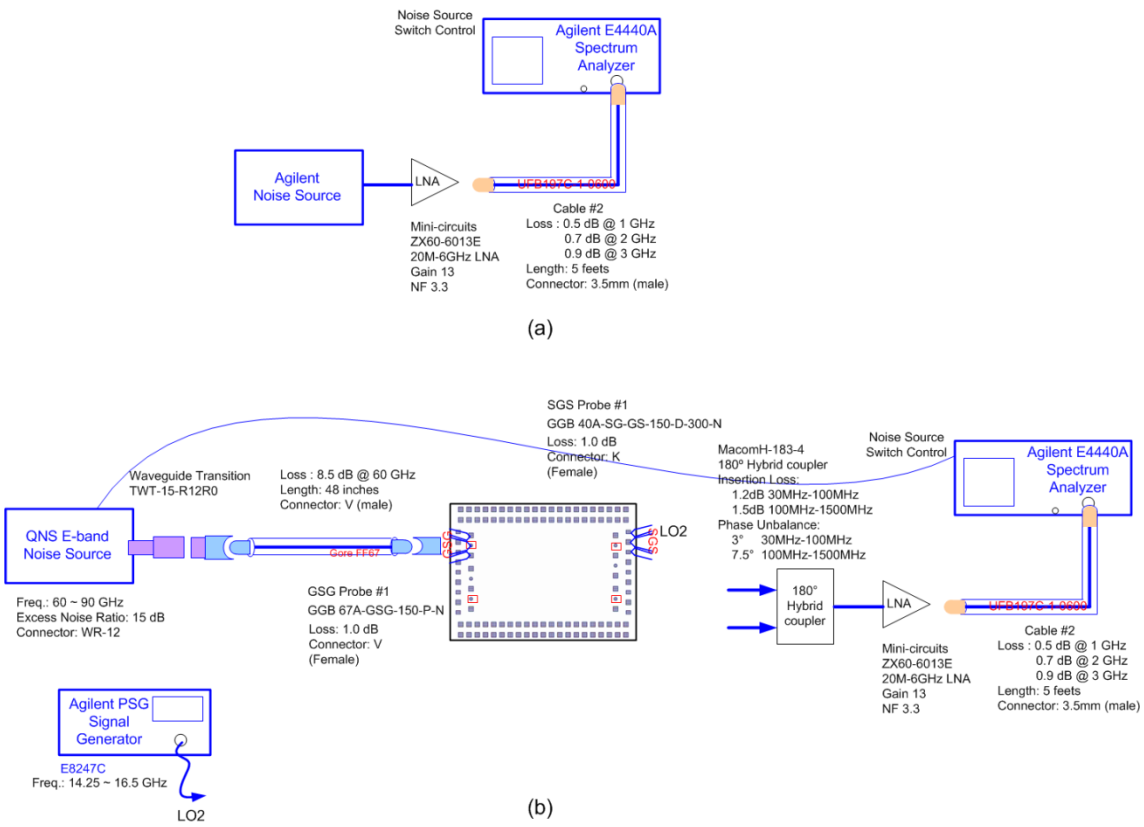

Fig. 8.13 Setup for noise figure measurement: (a) calibration, (b) measurement

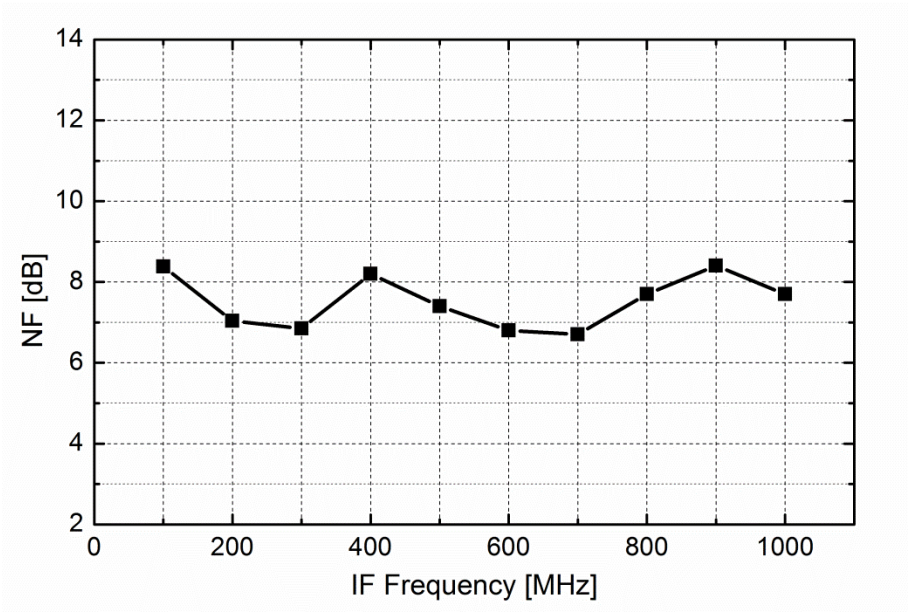

Fig. 8.14 Measured noise figure

As shown in Fig. 8.14, the noise figure is 7.4dB at IF frequency of 500MHz and the minimum value is 6.4dB.

8.5.5 Array Pattern

The system measurement setup is shown in Fig. 8.15.

The amplitude and phase errors are measured to be ±1.1dB and ±0.6°, respectively. Furthermore, the array pattern is synthesized. As shown in Fig. 8.16 and Fig. 8.17, one beam formed by all 4 elements has a peak-to-null ratio of 28.5dB.

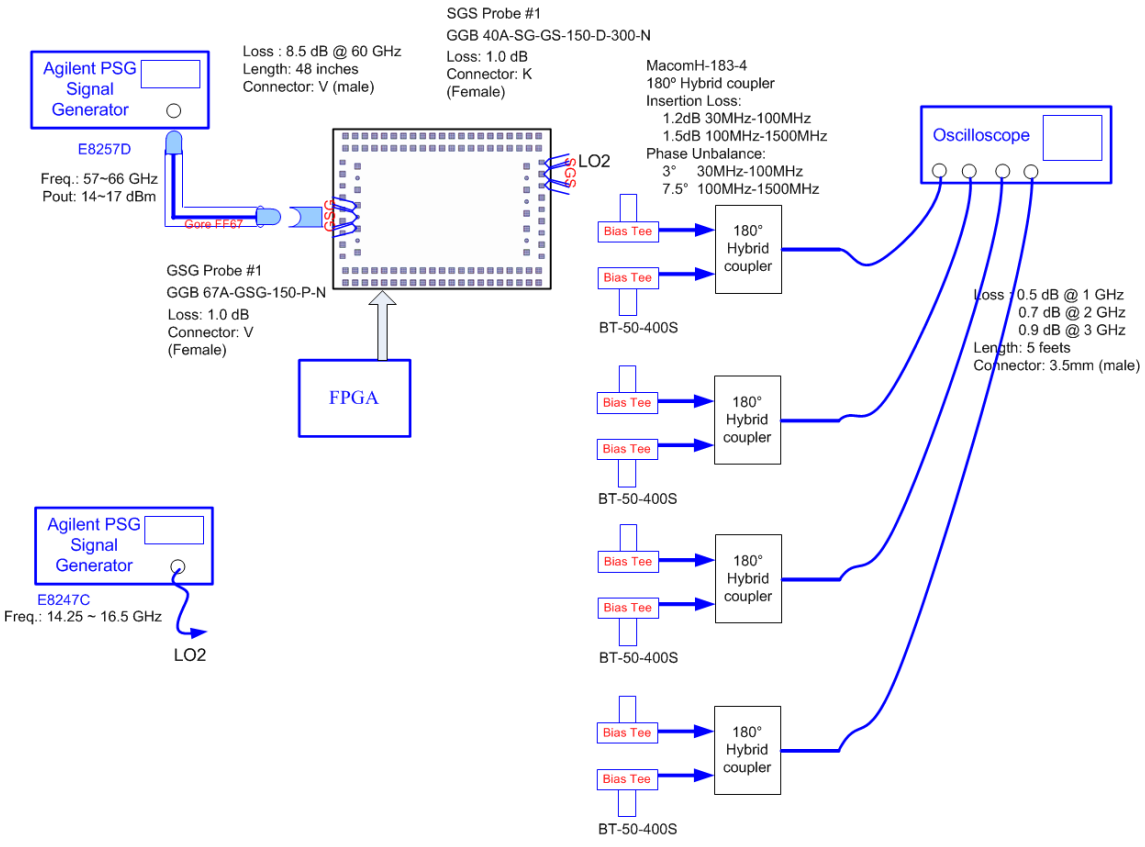

Fig. 8.15 Setup for array pattern measurement

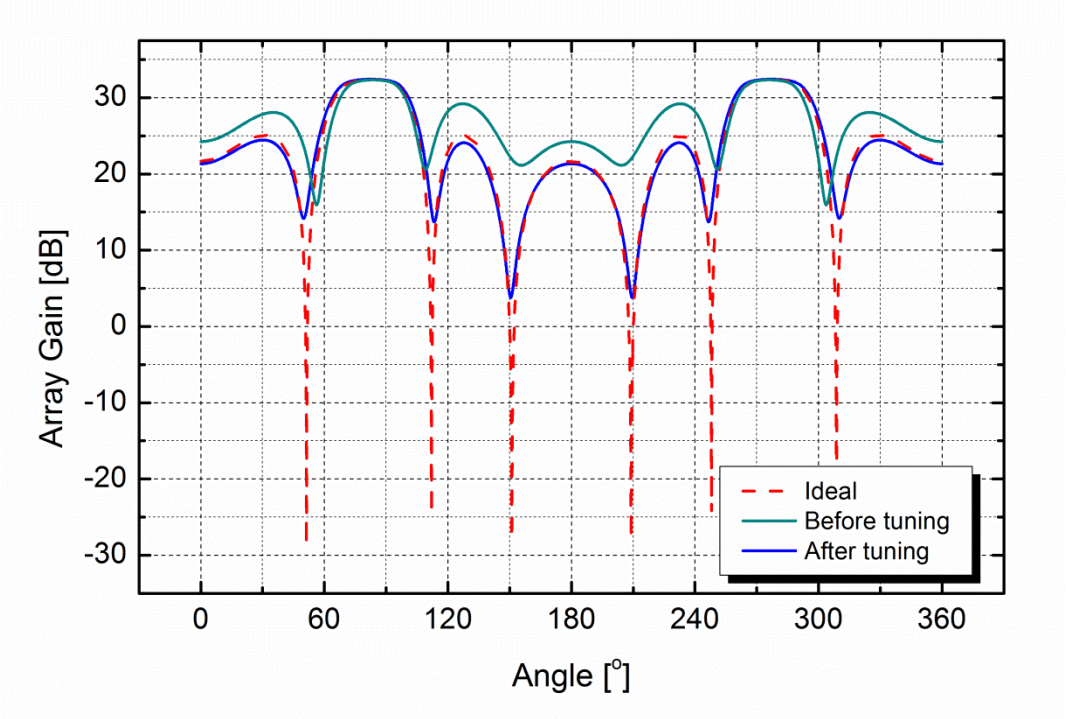

Fig. 8.16 Synthesized array pattern

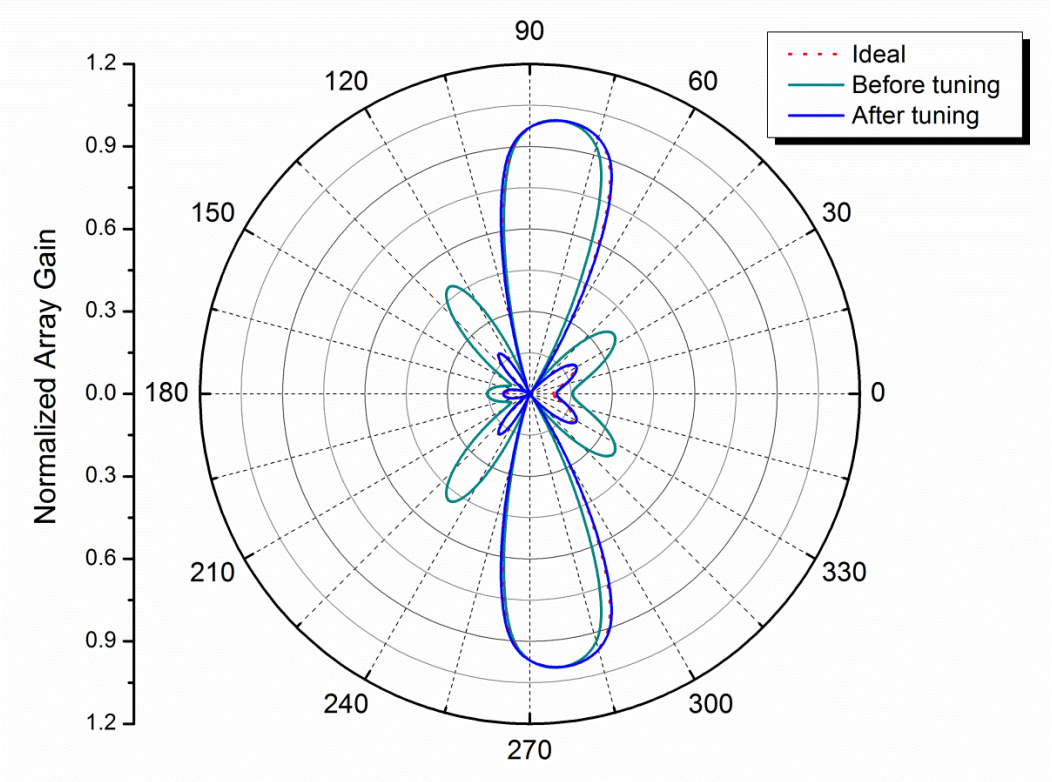

Fig. 8.17 Polar plot of synthesized array pattern

8.5.6 Statistical Result

Since the array pattern is very sensitive to process variations, two randomly picked samples have been measured. As shown in Fig. 8.18 and Fig. 8.19, the peak-to-null ratios of the first sample and the second sample are 28.5dB and 29.0dB, respectively.

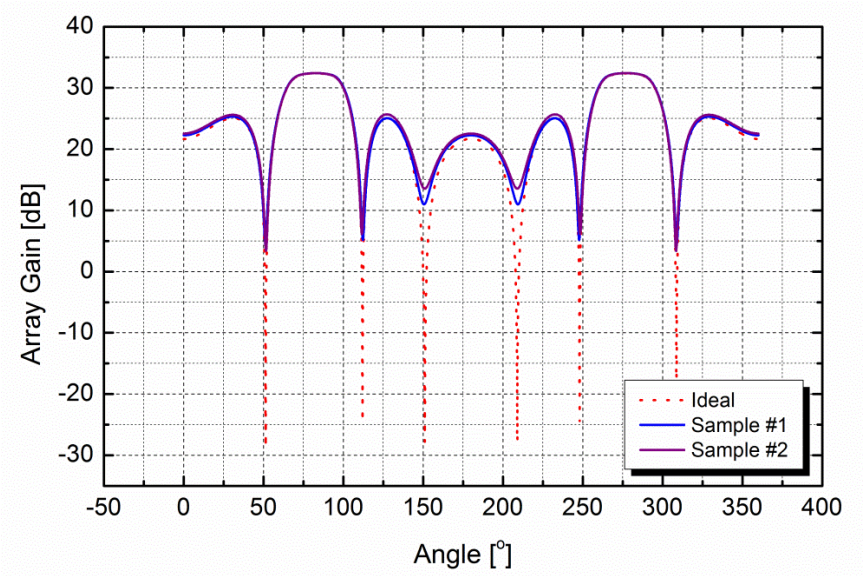

Fig. 8.18 Synthesized array patterns of two samples

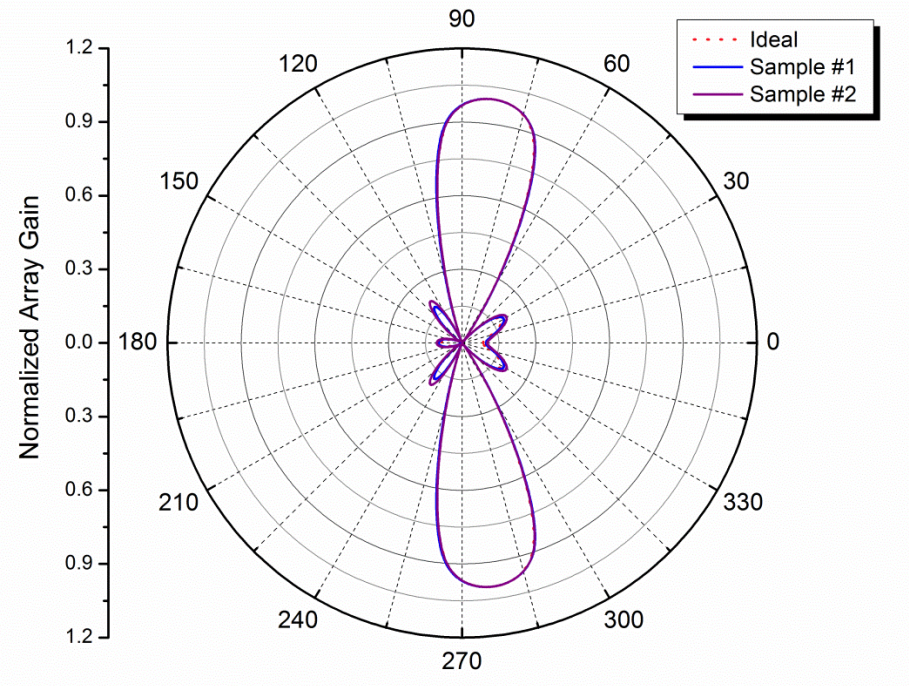

Fig. 8.19 Polar plot of synthesized array patterns of two samples

8.5.7 Performance Summary

The performance of proposed 4-path phased-array receiver summarized and compared with recently published 60-GHz receivers, as shown in Table 8.1.

Table 8.1 Performance summary and comparison of 60-GHz receiver

	Parameters	This work	[3]	[4]	[5]
	Frequency [GHz]	57.0 ~ 66.0	57.0 ~ 66.0	76.0 ~ 84.0	56.0 ~ 65.0
Per Element	**Voltage Gain [dB]**	21.0	39.0 *	33.0	24.0
	Noise Figure [dB]	6.5 ~ 8.4	6.5 ~ 7.3	11.5 ~ 13.5	6.3 ~ 7.5
	IP_{1dB} [dBm]	-12.5	-16.0	-21	-29.0
	Power [mW]	60	~ 306	75	27
	Area [mm^2]	0.65	1.51 **	1.99 **	0.68 **
Phased-Array	**Element Number**	4	16	16	4
	Phase Shifting	LO	RF	RF	Baseband
	Phase Resolution [°]	22.5	11.25	11.0	11
	Phase Error [°]	± 0.6	± 4	11.0	N/A
	Gain Error [dB]	±1.1	N/A	1.0	±1.1
	Peak-to-null ratio [dB]	28.5	N/A	N/A	30.0
	Close-loop Beamforming	Yes	No	No	No
	Total Power [mW]	320	1370	1200	137
	Supply Voltage [V]	1.2	2.7	2.0	N/A
	Technology	65nm CMOS	120nm SiGe BiCMOS	IBM 8HP SiGe BiCMOS	65nm CMOS

* VGA gain included

** Estimated from chip photo

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[1] L. Wu, A. Li and H.C. Luong, "A 4-Path 42.8-to-49.5GHz LO Generation with Automatic Phase Tuning for 60GHz Phased-Array Receivers," *ISSCC Dig. Tech. Papers*, pp.270-271, Feb. 2012.

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Chapter 9

Conclusion and Future Work

9.1 Summary

In this dissertation, system architecture and circuit techniques are investigated to realize a 4-path phased-array receiver RF front-end for IEEE 802.15.3c. Chapter 1 introduces the research background. Chapter 2 and Chapter 3 discuss the system specification, basic receiver architectures and phased-array receiver architectures. The general considerations and the specifications of the phased-array receiver are derived and summarized in Chapter 3.

Chapter 4, Chapter 5 and Chapter 6 presents some proposed techniques in circuit level for 60-GHz LO generation, including divider-by-4, QVCO and VCO.

In Chapter 4, a simple but effective locking range enhancement technique is proposed for LC-type divide-by-4 ILFDs at mm-Wave frequencies. By employing a 4^{th}-order LC tank with the two frequency peaks properly designed at ω_0 and $3\omega_0$, the 3^{rd}-order harmonic gets boosted that significantly enhances the injection efficiency and thus the locking range of divide-by-4 ILFDs. Implemented in 65-nm CMOS, the prototype measures a locking range of 21.9% from 58.53 to 72.92 GHz while consuming 2.2mW from a 0.6V-supply, which corresponds to an FoM of 6.54.

In Chapter 5, a transformer-based enhanced-magnetic-tuning technique is presented to tune the frequency of millimeter-wave oscillators. By switching the polarity of the

phase shift of the coupling currents, both of the two intrinsic modes in a quadrature VCO (QVCO) are exploited to achieve ultra-wide frequency tuning range. Designed and implemented in 65nm CMOS process, the QVCO with proposed bimodal enhanced-magnetic-tuning measures a continuous tuning range of 24% from 48.8 to 62.3 GHz and phase noise of -90 to -94 dBc/Hz at 1MHz offset while drawing 13 to 25 mA from 1.2-V supply, corresponding to FoM from 173 to 176 dBc and FoM_T from 181 to 184 dBc.

In Chapter 6, a dual-band millimeter-wave VCO is designed by exploiting the intrinsic multiple oscillation modes of a standing-wave oscillator. Implemented in 0.13μm CMOS with an area of 0.05mm^2, the VCO prototype measures a dual-band operation at 24 GHz and 60 GHz with tuning range of 10.8% and 7.2%, phase noise of -120dBc/Hz and -114dBc/Hz at 10MHz offset, power consumption of 11mW and 24mW, corresponding to FoM of -177dB and -176dB, respectively.

Chapter 7 and Chapter 8 focus on the system design and implementation of 4-path phased-array receiver, including both LO phase shift generation and RF front-end.

In Chapter 7, a 4-path LO generation with automatic successive phase tuning is proposed for mm-Wave phased-array receivers. Each LO path has a phase shifter based on injection-locked oscillator, a frequency tripler with enhanced locking range, and a 3rd-order standing-wave buffer. Implemented in 65nm CMOS, the prototype measures linear phase ranges larger than 180°, amplitude variation less than ±0.4dB, phase resolution of 22.5° between neighboring paths, and RMS error of 0.93° while drawing 85mA from 1V.

In Chapter 8, a 4-element phased-array receiver is designed and integrated. The RF front-end operates in hybrid-mode to improve linearity with little degradation of other

performance. Closed-loop beamforming by sequentially performing gain equalization, I/Q calibration and successive-approaching phase tuning is proposed and a peak-to-null ratio of 28.5dB has been achieved.

9.2 Contribution of the Dissertation

Firstly, based on theoretical analysis, a locking range enhancement technique by harmonic boosting is proposed to improve the performance of mm-Wave divide-by-4 injection-locked frequency divider.

Secondly, a locking range enhancement technique by enlarging the frequency conversion efficiency is proposed to improve the performance of mm-Wave injection-locked frequency tripler.

Thirdly, a bimodal enhanced magnetic tuning technique is proposed to improve the performance of QVCOs operating at high frequencies up to 60GHz. The associate theory of frequency tuning is developed.

Fourthly, dual-band operation for mm-Wave VCO is enabled by proposed standing-wave mode-switching technique, and its associated stabilization theory is developed.

Fifthly, a topology for variable linear phase shift generation is proposed and demonstrated.

Sixthly, virtual third-order standing-wave mode buffer is proposed to drive large capacitive load.

Seventhly, successive-approximation algorithm is proposed to automatically perform phase detection and tuning. Furthermore, closed-loop beamforming is achieved by proposed gain equalization followed by phase tuning.

Eighthly, hybrid-mode architecture is proposed to improve the performance of receiver RF front-end in terms of linearity, noise figure and gain.

Finally, the dissertation contributes the design, integration and measurement of the whole 4-path phased-array receiver system.

9.3 Potential Future Work

The main focus and contribution of this work are in the LO generation and RF front-end designs for 60-GHz receivers. Nevertheless, there are some potential topics worthy of further investigation.

On-chip antenna offers tremendous advantages as it reduces the chip-to-board design complexity and the associated cost for mm-Wave SoCs. In addition, antenna co-designed with LNA is expected to improve the system performance. However, the gain of the on-chip antennas is limited compared with off-chip ones and novel theories and techniques are mandated. Besides, the accurate characterization methodology for on-chip antenna is needed.

Another issue is the design and implementation of high-speed ADC and digital baseband. As the data rate significantly increases, the performance of ADC and digital baseband becomes very critical. Their associated large power consumption and large chip area will make the integration of mm-Wave phased-array SoC very challenging.

Except from IEEE 802.15.3c, there are some other standards such as ECMA 387, WirelessHD, 802.11.ad, Wireless Gigabit Alliance. How to implement a reconfigurable transceiver compatible with all of the standards would be interesting.

Appendix-I

List of Publications

Conference papers:

1. **Liang Wu**, Alan W. L. Ng, Lincoln L. K. Leung, and Howard C. Luong, "A 24-GHz and 60-GHz Dual-Band Standing-Wave VCO in 0.13μm CMOS Process," *Radio-Frequency Integrated Circuits (RFIC),* pp. 145-148, Jun. 2010.

2. **Liang Wu**, Alvin Li, and Howard C. Luong, "A 4-Path 42.8-to-49.5GHz LO Generation with Automatic Phase Tuning for 60GHz Phased-Array Receivers," *IEEE International Solid-State Circuit Conference (ISSCC), Dig. Tech. Papers*, pp. 270-271, Feb. 2012.

3. **Liang Wu**, and Howard C. Luong, "A 0.6V 2.2mW 58-to-73GHz Divide-by-4 Injection-Locked Frequency Divider," *IEEE Custom Integrated Circuits Conference (CICC),* Sep. 2012, to appear.

4. **Liang Wu**, and Howard C. Luong, "A 49-to-62GHz CMOS Quadrature VCO with Bimodal Enhanced Magnetic Tuning," *European Solid-State Circuits Conference (ESSCIRC),* Sep. 2012, to appear.

5. **Liang Wu**, Hiu Fai Leung, Alvin Li, and Howard C. Luong, "A 60-GHz CMOS 4-Element Phased-Array Receivers with Transformer-Based Hybrid-Mode Mixing and

Automatic Calibration," *IEEE International Solid-State Circuit Conference (ISSCC), Dig. Tech. Papers*, to be submitted.

Journal papers:

1. **Liang Wu**, Alvin Li, and Howard C. Luong, "A 4-Path CMOS 42.8-to-49.5GHz LO Generation with Automatic Phase Tuning for 60GHz Phased-Array Receivers," *IEEE J. Solid-State Circuits,* in preparation.

2. **Liang Wu**, and Howard C. Luong, "A V-Band Divide-by-4 Injection-Locked Frequency Divider with Locking Range Enhancement," to be submitted.

3. **Liang Wu**, and Howard C. Luong, "A Bimodal Enhanced Magnetically Tuned Quadrature VCO with 49-to-62GHz Tuning Range," in preparation.

4. **Liang Wu**, Hiu Fai Leung, Alvin Li, and Howard C. Luong, "A Fully Integrated 4-Path 60GHz Phased-Array Receivers RF Front-End in 65nm CMOS," to be submitted.

Patents:

1. **Liang Wu**, and Howard C. Luong, "A Successive-Approximation Algorithm for Automatic Phase Tuning," *US Patent,* to be filed.

2. **Liang Wu**, and Howard C. Luong, "Method for Frequency Tuning of Oscillators Based on Bimodal Enhanced Magnetic Tuning," *US Patent,* to be filed.